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High-Speed Bandwidth Acquisition System Based on Intermediate Frequency Signal Processing

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Abstract: In the high-speed bandwidth acquisition and playback system, due to the current hardware conditions, it is impossible to directly sample the signal at the RF end. Therefore, first complete the down-conversion in the RF module, reduce the signal to the intermediate frequency, and then realize the digitization of the intermediate frequency signal. In response to this problem, a field programmable logic array chip (FPGA) and AD9680 were selected to process the intermediate frequency signal. Use AD9680 to collect the mid-band pass signal with a center frequency of 750 MHz and a bandwidth of 400 MHz as a signal source for test verification, and then pass through a parallel multiphase digital down-conversion module to achieve spectrum shifting. It is verified by testing that the design can normally process the intermediate frequency signal, and the out-of-band suppression reaches 60 dB, which meets the design requirements, has high stability, and has high application value in engineering applications.

Keywords: Software radio; IF signal; Digital down-conversion; FPGA; AD9680

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1. Introduction

With the rapid development of modern digital communication systems, the amount of data that systems need to process is constantly increasing, and the demand for data is also growing [1]. Currently, high-speed signal transmission systems receive and transmit signals that have been modulated into radio frequency (RF) signals. According to the current level of integrated circuit development, it is not feasible to directly sample RF signals. A more mature solution is the digital intermediate frequency (IF) reception technology [2]. First, an analog RF down-conversion circuit is used to convert the RF signal into an analog IF signal, which is then digitized.

The digital signal processing performed in the digital IF section generally takes two forms: implementation using a dedicated signal processor (DSP) or using a Field-Programmable Gate Array (FPGA) [3]. Developing with a DSP is very convenient and can reduce the development process. It is generally believed that to achieve good signal filtering effects, 100 operations are needed per sampling point. However, DSPs execute instructions

in a single cycle, and when the data sampling frequency is high, the data transfer rate will also be high, making it difficult for DSPs to handle. On the other hand, FPGAs are very suitable for processing data with high transfer rates. They have abundant internal logic resources available for use, short internal delays, and parallel processing capabilities. When paired with high-frequency system clocks, they can achieve very high data processing speeds.

2. Design theory analysis

2.1. Bandpass sampling theorem

If researchers want to sample a baseband signal with a spectrum of (0, f_H), according to the Nyquist sampling theorem, the sampling rate f_S must be at least twice that of f_H. However, for the wideband signal required by this system (with a spectral range of f_L - f_H), if researchers still adopt a sampling rate greater than twice the highest frequency, it will waste a lot of unnecessary resources. As can be seen from the sampling theorem, the periodic extension of the sampled signal, if the chosen sampling frequency is inappropriate, will cause the extended spectrum to overlap with the original signal spectrum, making it difficult to recover the original signal. On both sides of the frequency band (f_L, f_H), there are extension components ($-f_H + mf_s$, $-f_L + mf_S$) and ($-f_H + (m+1)f_S - f_L + (m+1)f_L$) generated by sampling [4]. To avoid spectral aliasing, the condition in equation (1) must be satisfied.

$$\begin{cases} -f_H + mf_S \le f_L \\ -f_H + (m+1)f_S \ge f_H \end{cases} \quad (1)$$

Where *m* is an integer greater than or equal to 0. By synthesizing equation (1), the following can be obtained:

$$\frac{2f_H}{(m+1)} \le f_S \le \frac{2f_L}{m} (0 \le m \le N-1) \quad (2)$$

where *N* is the largest positive integer not exceeding $f_H|B$. According to the bandpass sampling theorem, when the signal being sampled is a high-frequency bandpass signal, the sampling frequency can be significantly reduced. However, applying the bandpass sampling theorem requires a prerequisite: the useful signal being sampled must reside within a single frequency band. If it appears in other frequency bands, it may lead to signal aliasing.

2.2. Parallel down-conversion filter structure

In modern digital communication systems, digital down-conversion (DDC) is a widely applied technology. Its primary purpose is to shift the signal spectrum downward to the desired frequency. Traditional digital down-conversion consists of three modules: the NCO (Numerically Controlled Oscillator), the mixing module, and the filter bank module [5]. However, the traditional digital down-conversion operates in a serial structure, which can impose a significant clock burden when the ADC sampling rate is too high, thereby affecting the stability of the entire system. When the AD sampling frequency is excessively high, a polyphase-structured digital down-conversion technique is generally employed for down-conversion operations, as illustrated in **Figure 1**. In this structure, data is input in parallel, and both the NCO and the filter bank are also structured in parallel. This approach meets the down-conversion requirements for high-speed ADC data acquisition without increasing the clock frequency.

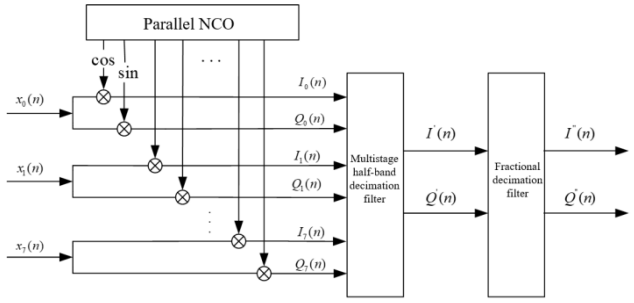

Figure 1. Parallel multi-phase digital down-conversion structure diagram

3. FPGA implementation of AD9680 acquisition

3.1. ADC device selection

The ADC device of this design requires that the number of quantization bits is not less than 14 bits, and the bandwidth of the signal is up to 400 MHz. The selection of ADC devices is carefully measured from three aspects: quantization bits, sampling frequency, and analog input bandwidth.

The signal collected in this design is divided into two types. The acquisition requires two channels. One collects a fixed 750 MHz medium frequency band communication signal, and the other collects a frequency of 1 M – 1 GHz. Among them, the 750 MHz center frequency signal has a maximum bandwidth of 400 MHz; the maximum bandwidth in the frequency range of 1 M – 1 GHz is 375 MHz, and the frequency range is 625 M – 1000 MHz. Moreover, the higher the sampling frequency, the better the suppression effect of the collected signal on the spectrum aliasing, and the maximum sampling rate needs to be greater than 1 GHz. By comparison, ADI's dual-channel analog-to-digital converter AD9680, whose maximum sampling frequency can reach 1.25 GHz, supports JESD204 B coded output and can be used for up to 2 GHz broadband analog signal sampling. Built-in on-chip buffers and sample-and-hold circuits are specifically designed for low power consumption, small size, and ease of use. The AD9680 core adopts a multi-stage differential pipeline structure, integrates output error correction logic, and uses an integrated reference power supply to simplify the design. Each ADC in the AD9680 integrates two DDCs, and the DDC module can complete filtering, down-conversion, extraction, and complex real number conversion. At the same time, the AD9680 also has AG, which can simplify the design of the receiver. It also has a flexible power-down option, which can significantly reduce power consumption when conditions permit. The above characteristics can be configured by three-wire SPI. **Figure 2** is the function block diagram of AD9680.

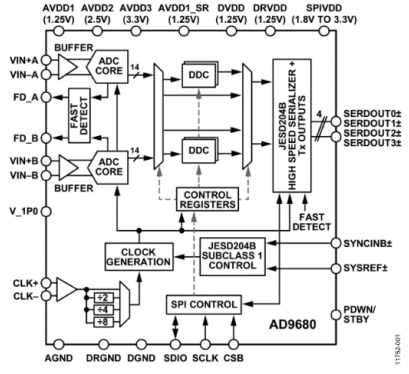

Figure 2. Functional block diagram for AD9680

3.2. AD9680 configuration and FPGA design

The AD9680 chip uses a three-wire SPI interface to read from and write to its internal registers. During the configuration process, the main tasks involve digital processing and JESD204B output settings.

The AD9680 is a dual-channel device, but its two channels are not used simultaneously. Therefore, the number of converters M is set to 1, the JESD204B word N' is set to 16, and an appropriate number of link lanes L is chosen as 4. Based on these parameters, the calculated lane rate for the AD9680 is 5 Gbps. The number of samples per frame parameter SS is typically set to an integer, often 1. In this design, to improve data transmission efficiency, the parameter SS is set to 2. After calculation, the number of bytes per frame parameter F for the AD9680 is determined to be 1, resulting in the JESD204B parameter LMFSLMFS for the acquisition link being 4112.

The AD9680 supports JESD204B Subclass 1, and during register configuration, the JESD204B link parameters within the chip need to be set. The chip manual also provides a quick configuration for register 0x570 based on the link parameters. When M=1, N'=16, and LMFS=4112, the value of register 0x570 must be set to 0x80. The default JESD204B lane rate for the AD9680 is 6.25 to 12.5 Gbps, but the calculated lane rate is 5 Gbps, so register 0x56E needs to be modified. Registers 0x5B2 to 0x5B6 control the mapping between JESD204B logical lanes and physical lanes, and the appropriate mapping is selected in coordination with the hardware circuit design. **Figure 3** shows the main flowchart of the AD9680 configuration program.

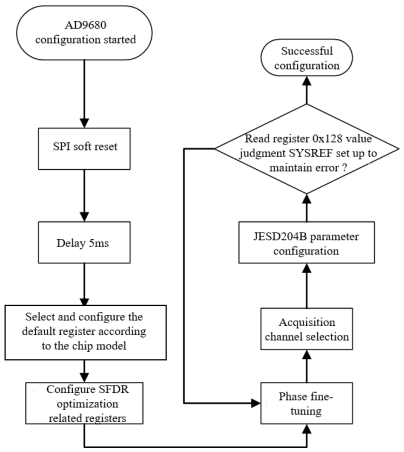

Figure 3. AD9680 configuration flow chart

Determine the registers and related parameters that AD9680 needs to configure, write the Verilog program, and after Vivado synthesis, the RTL diagram is shown in **Figure 4** below.

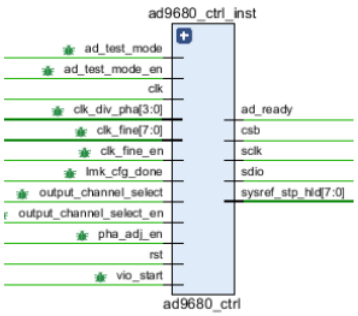

Figure 4. AD9680 configuration RTL diagram

4. Logical implementation of parallel polyphase down-conversion

4.1. Parallel link number conversion

The intermediate frequency signal collected by AD9680 is divided into four channels after JESD204 B demapping. If it is combined into one way to do down conversion, the clock frequency will become higher, and the FPGA chip will also be difficult to achieve this frequency. Therefore, the researchers choose to use resource exchange speed and parallel processing to complete digital down conversion.

When the demapping of the collected data is divided into 4 channels, to reduce the consumption of FPGA on-chip resources, 4 channels of signals need to be converted into 6 channels of signals. **Figure 5** is the RTL diagram of 4-way to 6-way.

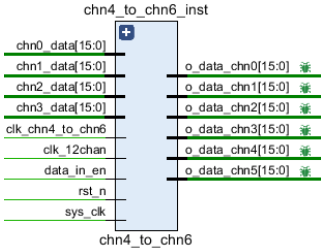

Figure 5. Parallel 4-way to 6-way RTL diagram

4.2. Parallel NCO implementation

If the researchers know $cos\,(2\pi f_c T_S * 6k)$,$sin\,(2\pi f_c T_S * 6k)$,$cos\,(\Delta\phi)$, and $sin\,(\Delta\phi)$, they can use the trigonometric formula to derive the expressions of the remaining paths.

In Simulink, the rotation module is designed according to the triangle formula, which consists of four multipliers, one adder, and one subtractor. Two NCO modules are designed to generate the first signal and phase difference. Then the signal is input to the previous phase rotation module, and the second signal output can be combined. The structure is shown in **Figure 6** ($\theta_0 = 2\pi f_c T_s * 6k$).

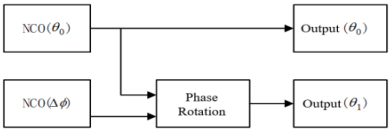

Figure 6. Simulink two NCO outputs

In the logic design, because there are multipliers and adders in the phase rotation module, there will be two clock delays between the input and output data. To ensure the last 6 data phases are similar, other signals can be obtained, and the top RTL diagram of the parallel NCO generation module is shown in **Figure 7**.

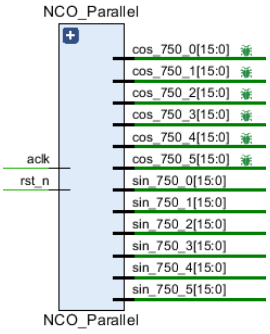

Figure 7. NCO generates the top-level RTL diagram of the module

4.3. Parallel FIR design

The filter structure of I and Q is exactly the same. The first is to use Simulink to design the required filter. In order to meet the out-of-band suppression of 60 dB and minimize resource consumption, 65 order filters are selected here to generate corresponding 66 filter coefficients. Then MATLAB divides the coefficients into 6 groups with 6 steps, 11 coefficients in each group.

Since the FIR IP core provided in Vivado will occupy more DSP resources, this design chooses to write FIR modules by itself. The parallel 6-channel I, Q signals are multiplied by the parallel carrier 6-channel I, Q signals as the input of the FIR module. The input signal is beaten, and then the FIR output signal of each channel is obtained by multiplying and adding with each channel coefficient. The Simulink construction of each FIR sub-module is shown in **Figure 8**, and the top-level RTL diagram of the parallel FIR module is shown in **Figure 9**.

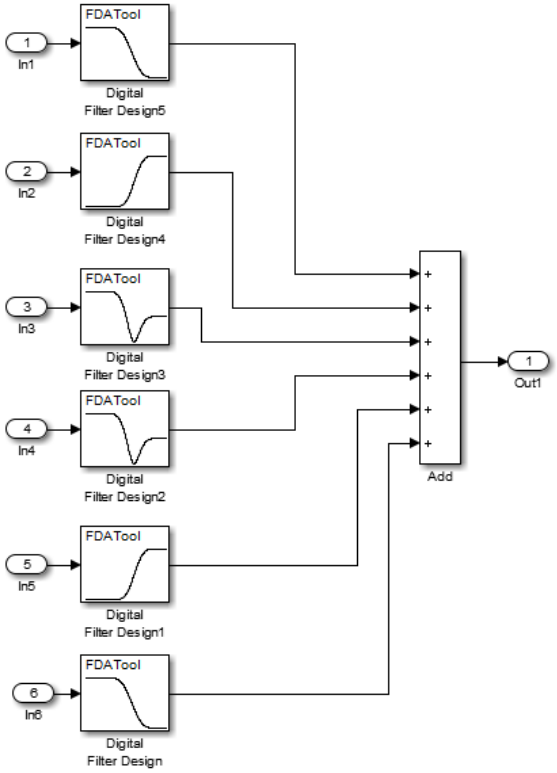

Figure 8. Simulink diagram of FIR submodule

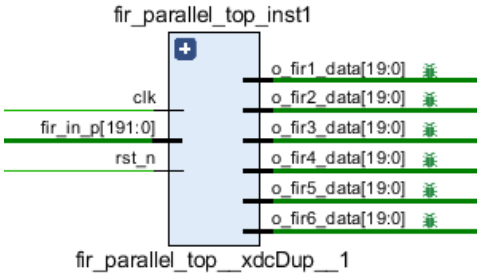

Figure 9. RTL diagram of FIR top-level module

5. Test verification

After the four 16-bit signals collected by the AD9680 are converted into six 16-bit parallel signals, they are multiplied by the six 16-bit of the parallel NCO module, and the obtained six data are sent to the parallel FIR module for filtering. The filtered data is intercepted to obtain six parallel FIR output data.

The FIR input data and output data are exported and analyzed in MATLAB. The sampling rate is 1GHz, and the spectrum diagram is shown in **Figure 10** and **Figure 11**, respectively. By comparing the spectrum of **Figure 10** and **Figure 11**, it can be seen that the filtering effect of the filter is better, and the out-of-band suppression reaches 60 dB, which meets the design requirements of this time. The abscissa is frequency / MHz, and the ordinate is amplitude / dB.

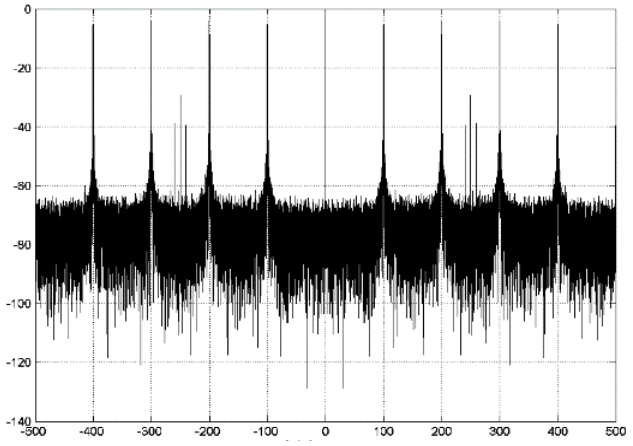

Figure 10. FIR input spectrogram

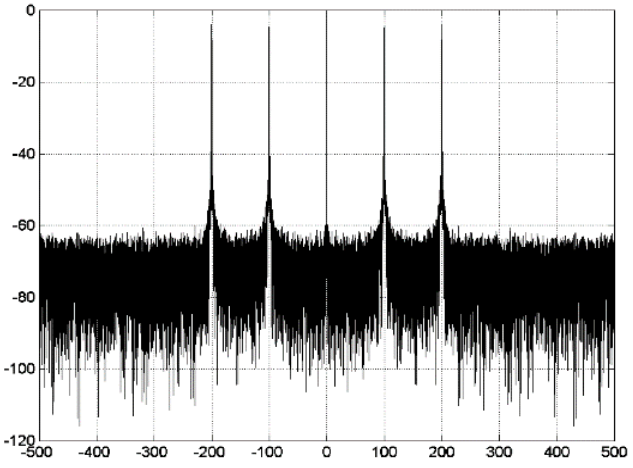

Figure 11. FIR output spectrogram

6. Conclusion

In this paper, an intermediate frequency signal processing based on FPGA and AD9680 is designed and successfully implemented. After testing and verification, this design can meet the parallel filtering of the band communication signal with a bandwidth of 400M and a center frequency of 750M, and achieve the design

requirement of 60dB out-of-band suppression. Compared with the traditional serial structure, this design has the characteristics of reducing clock frequency, improving system stability, and fast processing speed. The structure used in this design provides a more useful solution for intermediate frequency signal processing and has a high application value.

Disclosure statement

The authors declare no conflict of interest.

Author contributions

Study idea conceptualization: Ziming Yin
Experimentation: Ziming Yin, Yunyu Wei
Data analysis and paper writing: Ziming Yin, Kuo Wang

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