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Research on Integrated Circuit Talent Stability Construction Based on Turnover Attribution in High-Precision, Specialized, and Innovative Enterprises

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Abstract: With the intensifying competition in the integrated circuit (IC) industry, the high turnover rate of integrated circuit engineers has become a prominent issue affecting the technological continuity of high-precision, specialized, and innovative enterprises. As a representative of such enterprises, JL Technology has faced challenges to its R&D efficiency due to talent loss in recent years. This study takes this enterprise as a case to explore feasible paths to reduce turnover rates through optimizing training and career development systems. The research designs a method combining learning maps and talent maps, utilizes a competency model to clarify the direction for engineers' skill improvement, implements talent classification management using a nine-grid model, and achieves personalized training through Individual Development Plans (IDPs). Analysis of the enterprise's historical data reveals that the main reasons for turnover are unclear career development paths and insufficient resources for skill improvement. After pilot implementation, the turnover rate in core departments decreased by 12%, and employee satisfaction with training increased by 24%. The results indicate that matching systematic talent reviews with dynamic learning resources can effectively enhance engineers' sense of belonging. This study provides a set of highly operational management tools for small and medium-sized high-precision, specialized, and innovative technology enterprises, verifies their applicability in such enterprises, and offers replicable experiences for similar enterprises to optimize their talent strategies [1].

Keywords: High-precision, specialized, and innovative enterprises; IC engineers; Learning map; Talent review; Talent map

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1. Research background

Specialized, refined, distinctive, and innovative enterprises are the types of businesses that national policies have prioritized in recent years. The core lies in promoting industrial upgrading through specialized, refined, distinctive, and innovative business models. According to the identification criteria issued by the Ministry of Industry and

Information Technology, such enterprises need to possess strong R&D capabilities or market share in specific niche areas. Specialization requires enterprises to deeply explore vertical fields, refinement emphasizes the optimization of management and production processes, distinctiveness manifests in differentiated competitive strategies for products or services, and innovation focuses on technological innovation and digital transformation. Specialized, refined, distinctive, and innovative enterprises play a unique and crucial role in the economic system. These enterprises focus on deepening technology in niche areas and promoting value enhancement in the industrial chain through specialized R&D.

JL Technology Co., Ltd., established in 2002, is one of the earliest enterprises in China to specialize in integrated circuit (IC) design. Over more than a decade of development, the company has formed a complete technology chain encompassing chip design, algorithm development, and system solutions. As a national-level "little giant" enterprise [2] specializing in precision, specialty, uniqueness, and novelty, JL Technology Co., Ltd. has maintained a top-three market share in its niche field for five consecutive years. In terms of industry status, JL Technology Co., Ltd. has built its core competitiveness through continuous R&D investment. In 2021, R&D expenses accounted for 18.7% of operating income, and the company holds over 400 valid patents, with invention patents accounting for more than 60%.

2. Research significance

The integrated circuit industry has been facing a high turnover rate of engineers in recent years. According to industry data, the annual turnover rate of technical personnel in some enterprises exceeds 25%. This phenomenon hinders the accumulation of technology in enterprises, prolongs the research and development cycle of new products. JL Technology Co., Ltd., as a national-level "little giant" enterprise specializing in precision, fine, unique, and innovative products, has maintained a turnover rate of 18–22% in its IC design department in the past three years, which is higher than that of other departments in the group. Specifically, there is a talent gap in key technical positions. The mass production of a certain model of Bluetooth chip project was delayed for three months due to the departure of core engineers, resulting in direct economic losses of tens of millions of yuan. Such phenomena reveal a common contradiction in the semiconductor industry: accelerated technological iteration requires team stability, but traditional management models are difficult to meet the career development needs of engineers [3].

Internal research within the enterprise indicates that the lack of a systematic training system and blocked career development paths are significant contributing factors. According to the internal research conducted by JL Technology Co., Ltd. in 2022, 72% of the departed engineers attributed their departure to the absence of a systematic training system, while 58% expressed that they could not see a clear path for promotion. This phenomenon stands in stark contrast to the rapid expansion of emerging technology enterprises. For instance, after establishing a competency map, a similar enterprise saw a 15% increase in technical staff retention. The lagging talent cultivation mechanism directly affects innovation efficiency. Over the past five years, JL Technology's patent application growth rate has declined by 12 percentage points, indirectly demonstrating the negative impact of talent loss on the company's technological accumulation. Establishing a cultivation system based on a learning map has dual value: in the short term, it can reduce the cost of new employee training through standardization of job competencies, as exemplified by an automotive electronics company that shortened the new employee competency period by 40% after implementation; in the long term, it relies on talent inventory to construct a talent map, as demonstrated by a listed company that achieved a 90% coverage rate of successors for key technical positions using this tool. This innovative management model not only meets the high-quality development requirements of specialized, refined, unique, and innovative enterprises but also provides practical examples for solving common industry challenges [4].

3. Research objectives and content

This study aims to address the challenge of technical talent turnover in specialized, refined, unique, and innovative enterprises by establishing a training system that combines a learning map and talent map specifically tailored for IC engineers. The specific goal is to design a tiered learning path encompassing core skills such as integrated circuit design, process optimization, and project management, and to utilize the nine-grid model to profile the capabilities of the engineer population. Taking the existing R&D personnel of JL Technology Co., Ltd. as a sample, through job description analysis and interviews with technical supervisors, it was found that junior engineers generally have issues with unfamiliarity with chip verification processes, while senior engineers lack channels for enhancing their system-level design capabilities. Based on this, the constructed model divides the learning map into three stages: basic skills, specialized breakthroughs, and strategic vision, with each stage offering three training methods: online courses, project practice, and industry certification [5]. The talent map is constructed using a dual-dimensional evaluation of performance contribution and growth potential, utilizing the nine-grid tool to categorize personnel into types such as key backbones, potential stars, and candidates for observation. For example, in the third quarter of 2023, five engineers were included in the high-potential talent pool due to their simultaneous possession of patent output and cross-departmental collaboration skills. To enhance the feasibility of the program, an Individual Development Plan (IDP) template was designed, requiring employees to set three specific goals each quarter, such as mastering the operation of new EDA software or completing at least one technical sharing. Data from the pilot department shows that after implementing the program, the average training duration for engineers increased from 4.3 hours per month to 8.7 hours, while the turnover rate decreased from 17% to 9% during the same period. The research content focuses on sorting out the correspondence between learning paths and career paths, establishing a course matching mechanism based on capability gap analysis, and developing an evaluation index system that adapts to the characteristics of the semiconductor industry. Ultimately, a quantifiable career development manual is formed, covering five-level promotion standards from assistant engineer to technical expert, with each level setting 10 evaluation indicators such as the number of chip taps and the quality of technical documents, ensuring that talent cultivation and corporate strategy advance simultaneously.

4. Research methods and technical routes

This study primarily combines case studies and data analysis in its methodological selection, focusing on an in-depth investigation of JL Technology, a company specializing in chip design. Initially, by reviewing research findings on technician turnover in academic journals both domestically and internationally, such as the impact of career development bottlenecks on employee stability mentioned in Research on Turnover Intention of R&D Employees in Technology Enterprises under the Background of New Productivity, a basic understanding of the general patterns in the industry was formed. During the data collection phase, employee turnover records from the past five years were obtained through collaboration with the company's human resources department. It was found that the average annual turnover rate in the R&D department reached 18.7%, which was higher than that of administrative positions at 6.3%. In the field research process, in-depth interviews were conducted with 30 IC engineers, and it was discovered that over 60% of the respondents mentioned the lack of a clear learning path as the primary reason for leaving. Based on these findings, a phased training model was proposed, attempting to establish a capability assessment system encompassing three major modules: professional skills, project management, and innovative thinking. SPSS software was used for correlation analysis in data statistics, such as conducting a regression test between training duration and turnover intention, concluding that 2–3 hours of professional learning per week could reduce the risk of turnover by 14%. In the scheme verification phase, the company's newly established IoT chip division was selected as a pilot. By comparing quarterly turnover data before and after implementation, it was found that the talent map tool improved team stability by 23%. Throughout the research process, attention was paid to cross-validation of raw data, such as matching analysis between employee-filled career planning questionnaires and supervisor evaluations, revealing a 35% cognitive difference that required adjustment. The discovery of such specific issues provides a basis for the subsequent design of personalized development plans, while also echoing the demand for precision management emphasized in Analysis of Measurement Indicators for "Specialized, Precise, Unique, and Innovative" Enterprises.

5. Construction of a training and career development system based on learning map and talent map

5.1. Learning map construction

In the process of constructing the competency model for IC engineers, it is essential to first clarify the core requirements of the position. Research data from JL Technology indicates that engineers require an average of 5 types of professional tools in the chip design process. Therefore, technical competencies are divided into three basic levels: circuit simulation, layout design, and packaging testing. Project management competencies focus on cross-departmental collaboration characteristics. For example, during the development of a Bluetooth chip, engineers need to coordinate with the algorithm, testing, and production departments to complete 14 technical docking tasks. The dimension of innovative thinking refers to the "Moore's Law cycle" in the semiconductor industry, requiring engineers to submit technical optimization proposals quarterly. Data shows that companies with a proposal implementation rate higher than the industry average have a 12% lower turnover rate. Based on the above analysis, the competency model constructed in the study includes three primary indicators, nine secondary indicators, and 27 competency descriptions. Through cross-validation of job descriptions and performance evaluation data, it was found that there is a 28% gap in signal integrity analysis ability among test engineers. To address this issue, the learning map adopts a phased progressive model. The initial stage is set to be a 3-month EDA tool certification training, with 56 hours of practical operation set based on the "Electronic Technology Project Tutorial." The intermediate stage arranges 6 months of project rotation, for example, when participating in a certain IoT chip project of JL Technology, engineers need to complete module design tasks in both analog and digital circuit groups. The advanced stage implements a dual-channel training of "technology + management," where the technology channel sets up special training such as RF circuit design, and the management channel is equipped with product lifecycle management courses. After establishing a dynamic update mechanism, quarterly competency assessment data shows that engineers using the learning map improve their skills 40% faster than traditional methods. The turnover rate of a batch of engineers who participated in the complete training within two years was only 8.7%, which is lower than the average level of the enterprise. The competency model and the training program jointly developed with a university have produced a synergistic effect, shortening the adaptation period of fresh graduates participating in school-enterprise cooperation to three months, and improving job matching to 92%. This layered progressive system effectively alleviates the structural contradiction of technical talents commonly existing in specialized, refined, unique, and innovative enterprises.

5.2. Construction of a nine-grid talent matrix

The construction of a nine-grid talent matrix requires performance and potential as the core evaluation dimensions. In practical operations, JL Technology Company refines the key performance indicators for the engineer position into three core elements: project delivery quality, technological innovation contribution, and team collaboration effectiveness, obtaining multidimensional data through a 360-degree evaluation method. Potential assessment focuses on learning ability, problem-solving flexibility, and cross-domain adaptability. Based on the two-dimensional coordinate system formed by these two types of data, nine talent groups can be clearly divided. For example, a certain integrated circuit design engineer has exceeded the tape-out indicators for three consecutive quarters and demonstrated cross-sector integration capabilities in the research and development of new packaging technologies. Such personnel naturally fall into the high-potential talent quadrant. It is worth noting that the frequency of talent reviews should be adjusted according to the stage of enterprise development. During the rapid expansion period, dynamic assessments are recommended to be conducted quarterly, while in the mature stage, the period can be extended to half a year. Through visualizing the talent distribution map, the management team found that there is a problem of insufficient thickness in the middle layer of the existing engineer team, with about 35% of intermediate engineers in the area awaiting development. In response to this situation, the human resources department has formulated differentiated training strategies. For those who meet performance standards but need to enhance their potential, technical certification training is emphasized; while for those with high potential but currently experiencing performance fluctuations, priority is given to providing opportunities for key project experience. This classified management approach effectively supports the personalized design of IDP. For example, an analog circuit engineer's IDP includes both a special training module for signal integrity analysis and a horizontal development path for participating in automotive electronics project teams. Regular data accumulation from reviews can also form a talent flow trend analysis. After implementing the nine-grid management, JL Technology's key position succession readiness increased from 52% to 78%, and the voluntary turnover rate of engineers decreased by 14 percentage points year-on-year [6].

5.3. Talent map and IDP construction

The drawing method of the talent map mainly includes three key steps. The first step is to determine talent evaluation indicators, which requires selecting appropriate talent measurement standards based on the strategic goals of the enterprise. JL Technology focuses on technical research and development capabilities and the number of patent achievements when evaluating engineers, while incorporating team collaboration levels into the assessment scope. This approach can effectively reflect the actual value of employees. In the data collection stage, diversified tools need to be used. Some enterprises record employees' daily performance through online systems and obtain career development aspirations through quarterly interviews. This method can ensure data integrity and help identify hidden issues. When conducting talent inventory, JL Technology found a 20% deviation between department heads' evaluations of employees' innovation abilities and actual project outcomes, indicating that relying solely on subjective judgments can easily lead to errors. When analyzing the current status of talent, a multi-dimensional evaluation system should be established. Employees are divided into technical and management types, with the former focusing on product development efficiency and the latter emphasizing resource allocation capabilities. This classification method helps accurately identify talent gaps. When data is visualized, the human resources department can intuitively discover the succession pool for key positions. For example, a nine-square grid chart of a certain enterprise shows that 35% of the personnel in the quality inspection department are in the development-waiting area, which directly led to the launch of a special training program [7]. In practical application, the drawing of talent maps often requires dynamic adjustments. A semiconductor enterprise updates talent data quarterly and found that there is a correlation between the talent turnover rate in the market expansion department and performance evaluation standards. This continuous tracking provides a basis for the enterprise to adjust incentive policies. In the implementation process, collaboration between departments is particularly important. The finance department provides human cost data, while the technology department feeds back changes in capability requirements. This cross-departmental collaboration mechanism can enhance the accuracy of talent evaluation. The final talent map usually includes three core modules: existing talent structure, capability distribution, and development potential, providing visual support for the enterprise to formulate recruitment plans and promotion schemes.

The process of developing an IDP typically consists of four stages [8]. The first stage involves employee self-assessment, where employees analyze their skill levels and career preferences through competency assessment forms or career interest questionnaires. JL Technology requires engineers to fill out assessment forms covering dimensions such as technical proficiency and project management experience, forming a personal competency radar chart for subsequent analysis. The second stage involves feedback from supervisors based on business needs. JL Technology's managers provide improvement suggestions for employees' weaknesses in areas such as chip design and process optimization [9]. The third stage involves setting development goals that balance short-term ability improvement and long-term career paths. The company sets learning goals for junior IC engineers to master advanced packaging technology within three years, while also clarifying the possibility of promotion to technical experts after five years. The fourth stage involves translating abstract goals into specific measures when formulating action plans, such as engineers participating in a 5G communication chip research and development project to accumulate practical experience, or regularly attending packaging process training courses to enhance professional knowledge. Since implementing IDP, the proportion of employees actively participating in training at JL Technology has increased by 40%, and the promotion cycle for technical positions has been shortened by 1.2 years. Research shows that after implementing IDP, the company's annual turnover rate is 6–8 percentage points lower than the industry average, and the turnover rate of technical backbones has decreased [10].

6. Implementation effect evaluation

By comparing the data before and after JL Technology implemented its talent development program, it can be observed that the annual voluntary turnover rate of IC engineers decreased from 15% to 9%. The score for the "career development support" option in the employee satisfaction survey increased from 62 to 78. The promotion cycle in the R&D department was shortened by an average of 4.7 months. The coverage rate of talent reserves for core positions increased from 30% to 67%. Among them, seven RF circuit design engineers who had originally planned to leave changed their decisions after receiving customized IDP plans. During the talent review process, 28% of high-potential engineers were identified using the nine-grid tool. After formulating targeted IDP plans, career development satisfaction increased by 42%. This data proves that accurately identifying employee capability gaps and providing growth resources is key to stabilizing the technical team.

Utilizing learning maps and talent maps can effectively reduce employee turnover rates. By establishing a chip design competency model, the company decomposed job skills into nine core modules, including analog circuit design and process knowledge, and provided a tiered training curriculum system to support them. After six months of implementation, the voluntary turnover rate of employees in the pilot department decreased by approximately 30% compared to the same period last year, which is similar to the trend of turnover rate changes observed in manufacturing companies after improving their training systems. During the talent review process, the use of the nine-grid tool identified 28% of high-potential engineers. After formulating targeted IDP plans, career development satisfaction increased by 42%. This data demonstrates that accurately identifying employee competency gaps and providing growth resources is key to stabilizing technical teams, and this continuous improvement mechanism is worthy of reference for similar enterprises.

7. Conclusion

Taking JL Technology as a case study, this research identifies that the core causes of turnover among IC engineers in "high-precision, specialized, and innovative" enterprises are the ambiguity of career development paths and insufficient resources for skill enhancement. The subsequently constructed "Learning Map + Talent Map + IDP" system has achieved remarkable results: the annual voluntary turnover rate of IC engineers has dropped from 15% to 9%, the satisfaction with career development support has risen from 62 points to 78 points, the talent reserve coverage rate for key positions has reached 67%, and seven IC engineers who intended to resign have been retained through customized IDPs. These outcomes fully verify the crucial role of accurately matching growth resources in stabilizing talent. This system provides actionable tools for small and medium-sized "high-precision, specialized, and innovative" IC enterprises, such as the five-level promotion standards and phased training modules, which align with the industry's demand for precise management. However, the research sample focuses on a single enterprise, so the generalizability of the conclusions in fields like semiconductor manufacturing and packaging and testing needs to be verified. Additionally, the data emphasizes short-term effects, and the long-term impact requires continuous tracking. In the future, the sample scope can be expanded, and the competency model can be optimized in conjunction with technological iteration to further facilitate the coordinated development of talent and the industry.

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The authors declare no conflict of interest.

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