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# Research on π/4QPSK Modulation Communication Transmission System and FPGA Implementation

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**Abstract:** This paper examines the π/4QPSK modulation communication transmission system, analyzing the performance advantages and disadvantages of π/4QPSK in comparison to QPSK. It also presents a comprehensive FPGA implementation scheme for a modulation communication transmission system, integrating RS channel coding, framing, frequency conversion, and other modules. This design is based on practical research and development requirements. The Xilinx Spartan6 chip board was used for board-level verification. The π/4QPSK modulated signal was transmitted via D/A conversion and radio frequency, with the transmitted waveform was looped back for reception. After A/D processing, the correctness of the designed modulation transmission scheme was verified.

**Keywords:** π/4QPSK modulation; FPGA

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## 1. Introduction

In communication systems, the transmitter primarily consists of modules such as modulation, encoding, and framing. The design of the transmitter's signal directly affects the performance of the entire communication system. Digital modulation primarily involves mapping signals to constellation points, with different types of constellation diagrams directly affecting the system's noise resistance and the bandwidth resources it consumes. $\pi/4$ Quadrature Phase Shift Keying ($\pi/4$QPSK) combines the advantages of Quadrature Phase Shift Keying (QPSK) and Offset Quadrature Phase Shift Keying (OQPSK), making it a form of quadrature phase shift keying modulation. The constellation diagram of QPSK modulation can experience phase jumps of up to $\pi$, which can lead to spectral expansion and larger side lobes, as well as being affected by the nonlinearity of power devices. In contrast, OQPSK limits phase jumps to $\pi/2$, resulting in less bandwidth usage and better anti-interference capabilities, but with higher implementation complexity. $\pi/4$QPSK limits phase jumps to $\pi/4$ and $3\pi/4$, with minimal phase changes, making the spectrum more compact after filtering and limiting compared to the previous two. This results in better bandwidth utilization under small-scale fading conditions. Single-carrier systems have a

lower peak-to-average power ratio compared to multi-carrier systems, reducing the requirements for RF devices. Therefore, in communication systems with low throughput, such as messaging systems, or in systems with high real-time requirements, such as voice systems, single-carrier systems provide significant cost and overhead advantages. Thus, research on π/4QPSK communication systems is necessary.

π/4QPSK employs differential encoding, allowing for both coherent and non-coherent demodulation (differential demodulation). Non-coherent demodulation does not require the recovery of a local carrier, significantly reducing the impact of carrier synchronization inaccuracies on the system [1,2]. Additionally, non-coherent demodulation enables rapid synchronization, reducing the need for synchronization codes in the frame structure compared to coherent demodulation, thereby increasing the proportion of effective data and improving spectral efficiency. In fast-fading channels, differential demodulation can achieve lower bit error rates than coherent demodulation. However, π/4QPSK also has drawbacks, such as the need for linear power amplifiers and the potential loss of paired symbols in the event of reception errors [2]. Considering the trade-offs between the advantages and disadvantages of π/4QPSK modulation, it is suitable for burst wireless communication systems. In a study conducted by Zhou, π/4QPSK modulation was applied to ship communication systems to improve bandwidth efficiency and system flexibility [3]. As for Liu *et al.*, a lookup table method was used to synthesize π/4QPSK waveforms through multiple square-root raised cosine filters, achieving simpler implementation with minimal performance loss [4]. Zhou *et al.* proposed a cross-product frequency discriminator demodulation method to address frequency offset issues in burst transmissions of π/4QPSK [5]. The literature mentioned above primarily analyzes π/4QPSK from an algorithmic perspective, whereas this paper validates the system's transmission scheme through the FPGA implementation of the π/4QPSK transmitter.

## 2. π/4QPSK modulation transmitter implementation scheme

As shown in **Figure 1**, the transmitter of the π/4QPSK modulation system mainly consists of RS encoding, framing, serial-to-parallel conversion, differential encoding, and up-conversion modules. The transmitted signal is finally output through a DAC, resulting in the RF output of the π/4QPSK modulated waveform.

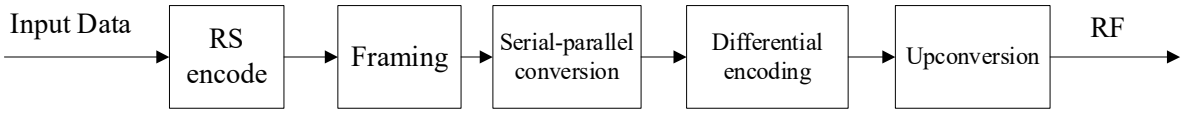


**Figure 1.** π/4QPSK modulation system

Reed-Solomon (RS) coding is a powerful forward error correction code suitable for correcting burst and random errors. It treats the original data symbols as polynomial coefficients and attaches a generator polynomial to the original data to form the encoded codeword. Therefore, RS coding has low overhead and implementation complexity, making it suitable for π/4QPSK systems. As shown in **Figure 2**, the RS encoder is implemented using a linear feedback shift register structure, with a division-based structure. The input consists of *m* original data symbols representing polynomial coefficients, and the generator polynomial is defined as $g(x) = (x-\alpha)(x-\alpha^2)...(x-\alpha^{2t})$, where α is the primitive element of the finite field $GF(2^m)$. After passing through this linear feedback shift register system, the output is the codeword.

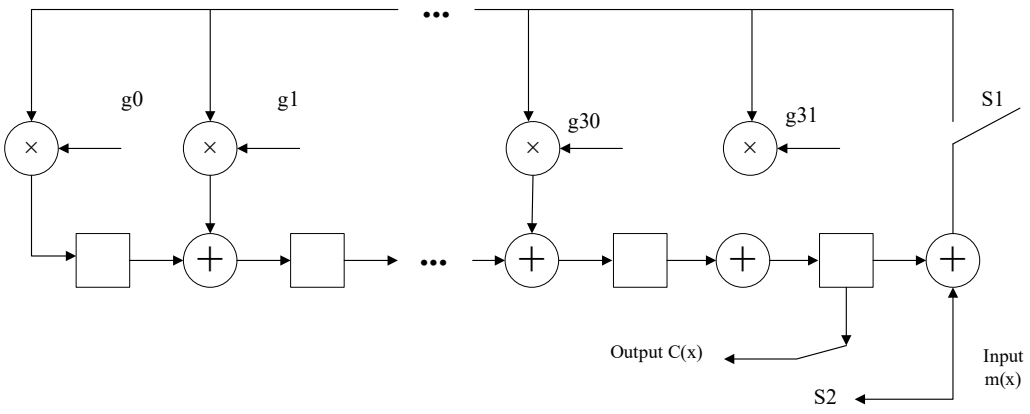


**Figure 2.** RS encoder structure

Since synchronization and other processing are required at the receiver, preamble symbols such as frame headers and synchronization frames (used by the receiver to detect the signal) are added to the output of the RS encoder. The final framed output remains a serial bitstream.

The serial-to-parallel conversion module maps the bitstream into I and Q signals, which are then fed into the $\pi$/4QPSK module. $\pi$/4QPSK modulation uses eight different carrier phases to represent digital information, as shown in the signal space diagram in **Figure 3**. The eight phase states are $\{0,\ \pi/4,\ \pi/2,\ 3\pi/4,\ \pi,\ -3\pi/4,\ -\pi/2,\ -\pi/4\}$. These phase states can be viewed as two sets of QPSK signal phases, with the black solid points forming one set $\{0,\ \pi/2,\ \pi,\ -\pi/2\}$ and the white hollow points forming the other set $\{\pi/4,\ 3\pi/4,\ -3\pi/4,\ -\pi/4\}$. The phase state transitions in $\pi$/4QPSK can only occur between these two QPSK phase groups, meaning the maximum phase jump in $\pi$/4QPSK is $3\pi$/4. The differentially encoded data is then up-converted and mixed before being sent to the DAC, resulting in the final transmitted $\pi$/4QPSK modulated signal.

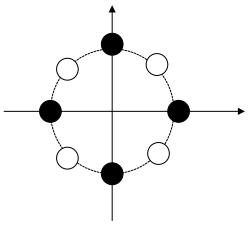

**Figure 3.** $\pi$/4QPSK constellation diagram

## 3. FPGA implementation of the transmitter

This paper uses the Xilinx Spartan6 FPGA hardware platform to implement the $\pi$/4QPSK modulation transmitter. The FPGA platform, equipped with hardware description languages, implements signal processing algorithms by building digital circuits, offering real-time processing, parallelism, and flexibility, making it suitable for communication systems. The FPGA platform can support multiple modulation schemes, data rates, and flexible waveform configurations. The $\pi$/4QPSK modulation transmitter scheme designed in this paper was verified through simulation on the Vivado platform and waveform debugging using Chipscope. The simulation and measured waveform analyses are as follows:

As shown in **Figure 4**, the simulation results of the RS encoder's input and output are presented. The input

data (datain) and output data (dataout) are shown, with the encoded results sequentially appended to the input data. The encoded output is available in the next clock cycle, verifying the low encoding delay. The input data length is 16 bytes, and the encoded output length is 32 bytes, achieving RS(32,16) encoding.

As shown in **Figure 5**, the simulation results of the framing module are presented. The output (data_bit) is the framed bitstream, combining the synchronization frame, frame header, and encoded data into a serial bitstream.

As shown in **Figure 6**, the simulation results of the modulation module are presented. The I and Q signals are the differentially encoded outputs, and the I and Q signals after shaping filtering and up-conversion are shown. The final synthesized I and Q signals are output as the modulated signal. The bitstream enters the modulation module, is converted into I and Q signals through serial-to-parallel conversion, and then differentially encoded. The differentially encoded I and Q signals undergo shaping filtering. A DDS generates a 25 MHz carrier, which is multiplied with the shaped I and Q signals. The resulting I and Q signals are summed to produce the final modulated output signal.

The final modulated $\pi$/4QPSK signal is output through a DAC and looped back into the hardware board. The waveform after A/D processing is shown in **Figure 7**, which represents the observable measured data waveform. The waveform is clear with minimal glitches, demonstrating that the designed transmitter hardware implementation meets practical application requirements.

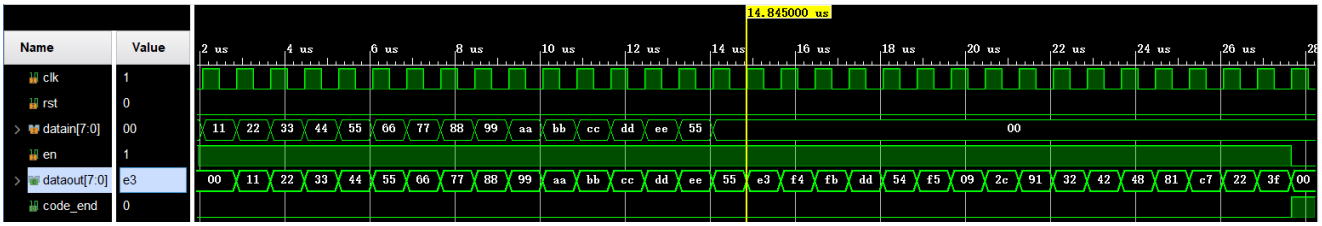


**Figure 4.** RS encoding simulation results

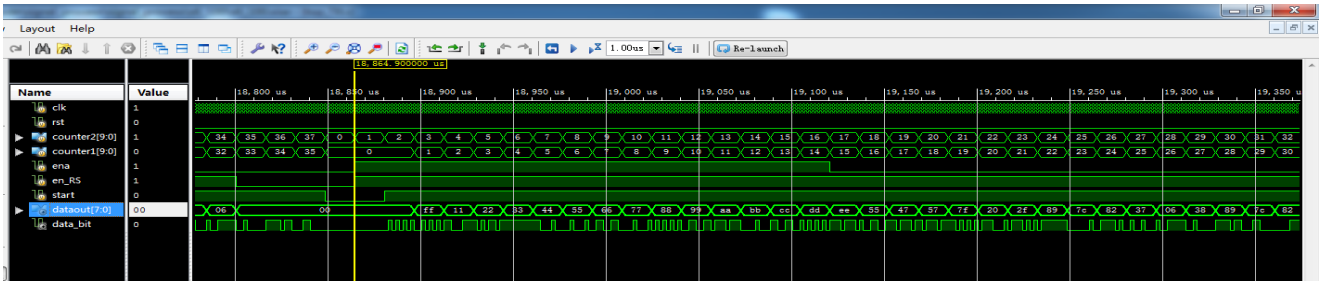


**Figure 5.** Framing module output simulation results

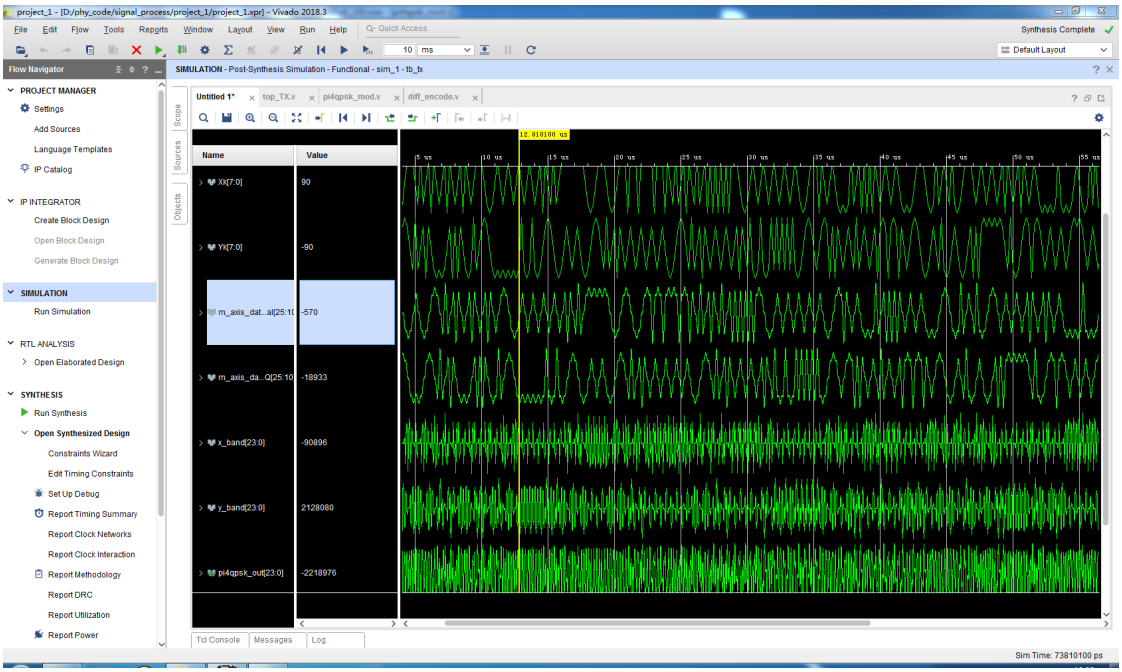

**Figure 6.** Modulation output simulation results

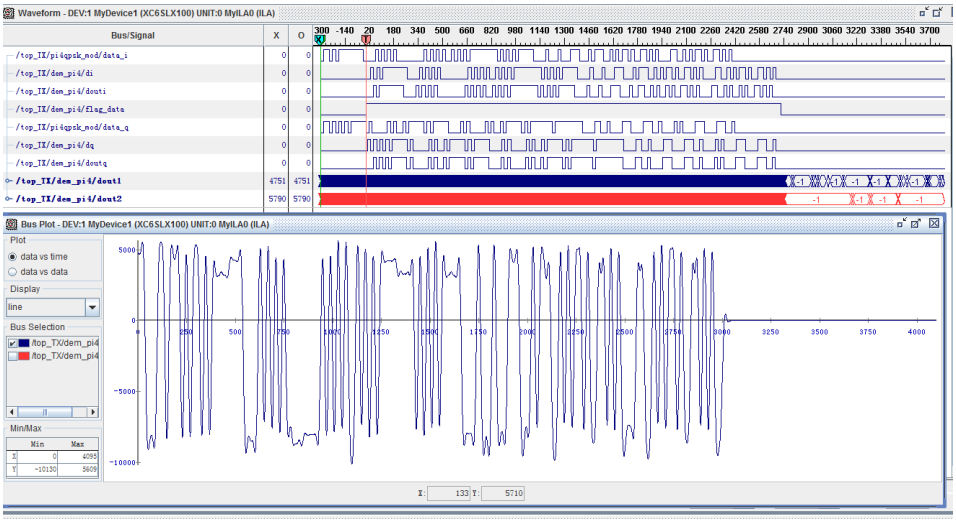

**Figure 7.** Measured waveform after D/A output and A/D input

## 4. Conclusion

This paper primarily introduces the simulation and FPGA implementation of the $\pi$/4QPSK modulation system, specifically including the implementation of RS encoding, framing, serial-to-parallel conversion, differential encoding, and up-conversion. The specific implementation methods for each module are discussed and the proposed methods are realized on the FPGA platform. By utilizing debugging software to observe the output signals and the outputs of each module, satisfactory results have been achieved.

## Disclosure statement

The authors declare no conflict of interest.

## Author contributions

Conceptualization: Yunjie Yuan
Investigation: Yuhui Chu, Xiaolei Cai
Formal analysis: Yanyan Wang, Peijie Yin
Writing: Yuhui Chu

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