Journal of Electronic Research and Application, 2025, Volume 9, Issue 4
http://ojs.bbwpublisher.com/index.php/JERA
ISSN Online: 2208-3510
ISSN Print: 2208-3502

A "Tonebusting" Technique to Build a DAC from a First-Order Digital ΣΔ Modulator

Yves Leduc, Gilles Jacquemod, Yoann Charlon*, Fabrice Muller

Université Côte d'Azur, Polytech'Lab, UPR UniCA7498, Sophia Antipolis, France

***Corresponding author:** Yoann Charlon, yoann.charlon@unice.fr

Abstract: In this paper, we present a novel first-order digital ΣΔ converter tailored for digital-to-analog applications, focusing on achieving both high yield and reduced silicon estate. Our approach incorporates a substantial level of dithering noise into the input signal, strategically aimed at mitigating the spurious frequencies commonly encountered in such converters. Validation of our design is performed through simulations using a high-level simulator specialized in mixed-signal circuit analysis. The results underscore the enhanced performance of our circuit, especially in reducing spurious frequencies, highlighting its efficiency and effectiveness. The final circuit exhibits an effective number of bits of 13.

Keywords: First-order digital SD modulator; Digital to analog converter; Spurious frequencies; Dithering

Online publication: August 7, 2025

1. Introduction

We aim to leverage the high density of digital circuitry to streamline the complexity of the analog component in a Digital-to-Analog Converter (DAC). Our approach involves utilizing a digital first-order Sigma-Delta (ΣΔ) modulator, which necessitates minimal analog filtering, along with a 1-bit output to circumvent the need for precise analog element matching. As a result, it ensures a substantial yield, but first-order Sigma-Delta DACs are notorious for producing prominent spurious frequencies [1].

Figure 1 illustrates the topology of such a DAC, while **Figure 2** displays the output signal spectrum prior to the low-pass filter for a 16-bit sinusoidal digital input with a frequency of 5kHz, an amplitude of -20dB peak, the sampling frequency being 16MHz. This result, as the following in this paper, has been done using NAPA, a high-level simulator specialized in mixed-signal circuit analysis [2].

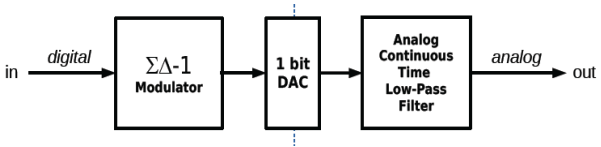


Figure 1. Topology of a first-order ΣΔ DAC

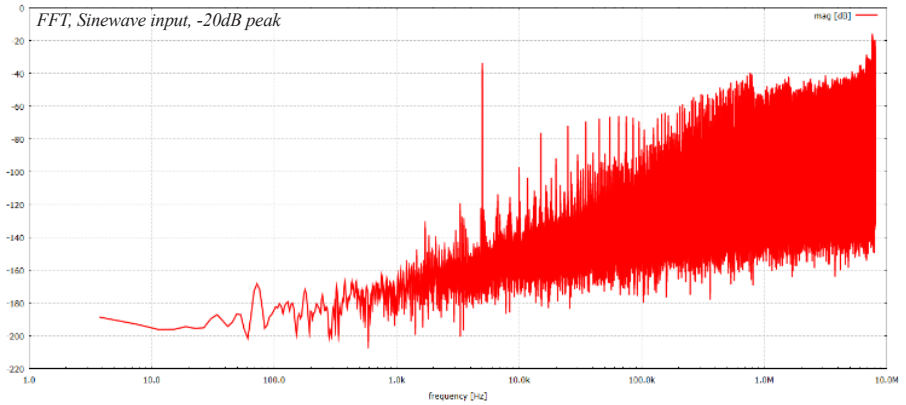


Figure 2. Output spectrum of the modulator showing parasitic oscillations

The presence of numerous spurious frequencies in the signal renders it challenging to distinguish between its modulation and spurious tones. Consequently, first-order ΣΔ modulators are unsuitable for various applications. In response, we introduce a novel topology for a first-order ΣΔ DAC designed to mitigate these spurious frequencies. Our approach involves the injection of high-level noise (dithering) into the input signal, as depicted in **Figure 3**.

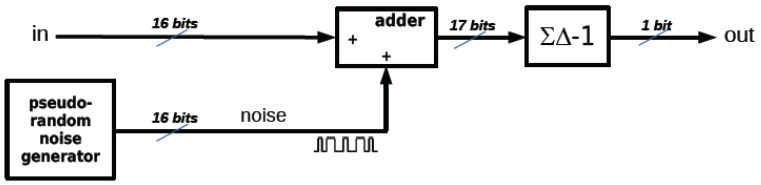


Figure 3. Topology of the first-order ΣΔ modulator with dithering

Part 2 is focused on the first-order digital ΣΔ modulator with dithering. Part 3 presents the analog DAC front-end, including the low-pass filter and the final simulation. A conclusion ends this paper.

2. Improved first-order digital ΣΔ modulator with dithering:

We chose to employ a simple digital pseudo-random noise generator (PRNG), Marsaglia's xorshift_32 bits [3]. This PRNG has the distinctive advantage of not requiring any multiplier while offering very good performance.

A heavy dithering noise is introduced into the input signal prior to the first-order SD modulator. As anticipated, the previously observed spurious frequencies are effectively suppressed, as illustrated in **Figure 4**. Notably, the amplitude of the noise far exceeds that of the signal, leading to this significant reduction in spurious frequencies.

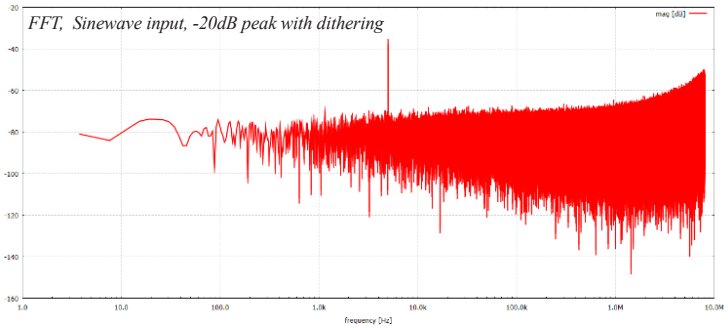


Figure 4. Output spectrum of the modulator with heavy dithering

Clearly, the noise level is unmanageably high, making signal restoration unfeasible. To tackle this issue, we propose the following architecture employing twin modulators in parallel (refer to **Figure 5**) to efficiently suppress this output noise as per Equation 1.

(signal + noise) + (signal - noise) = 2 x signal (1)

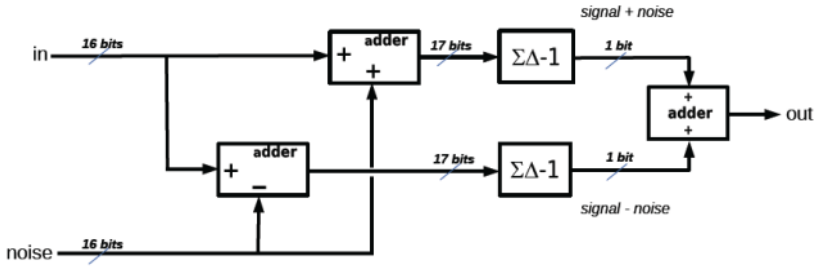


Figure 5. Topology of the first-order ΣΔ twin modulator with dithering

Due to the addition of two 1-bit signals, this initial topology fails to produce a 1-bit output. As a result, we choose to replace the final adder with a multiplexer, effectively doubling the output sampling frequency as depicted in **Figure 6**.

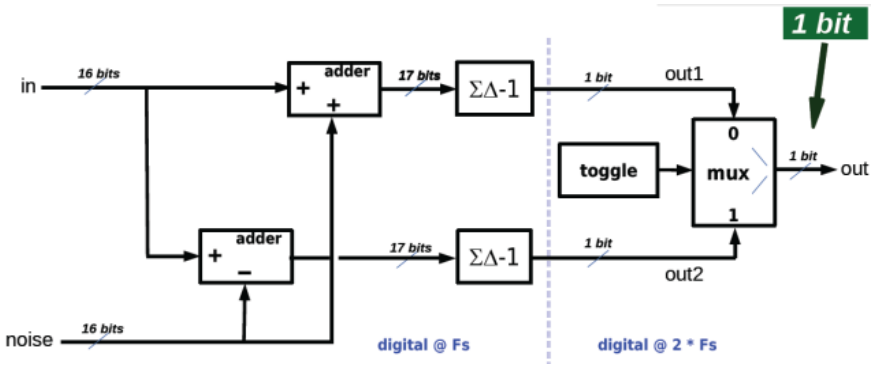


Figure 6. Final topology of the 1-bit first-order ΣΔ twin modulator

The output spectrum, for a -20dB peak and 5kHz input signal, is given in **Figure 7**. As expected, both spurious frequencies and dithering noise are removed.

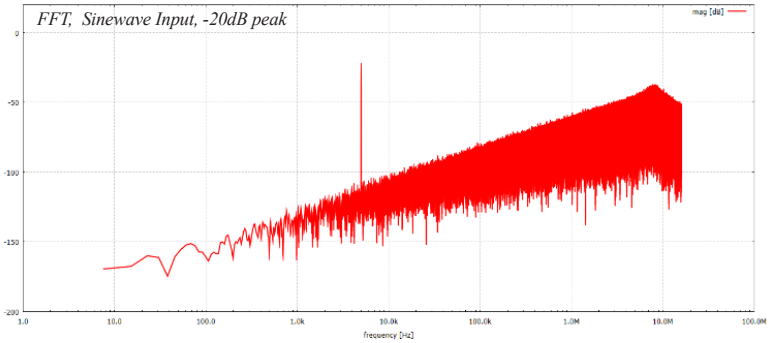


Figure 7. Output spectrum of the 1-bit first-order *ΣΔ* twin modulator

3. The analog DAC front-end

To reconstruct the analog signal, we employ an analog front-end, a 1-bit DAC followed by a low-pass filter, depicted in Figure 8.

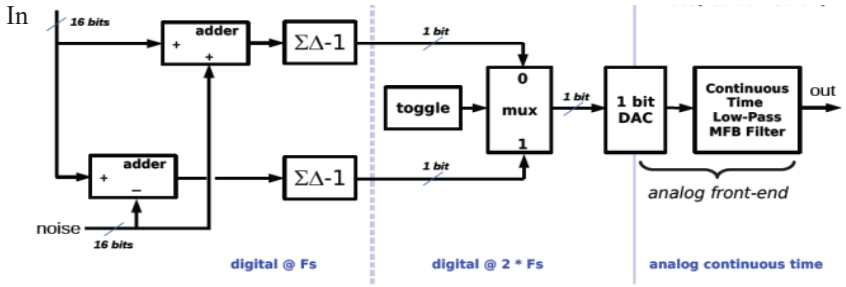


Figure 8. Final DAC architecture

The 1-bit DAC can be realized using a straightforward CMOS inverter, as illustrated in **Figure 9**.

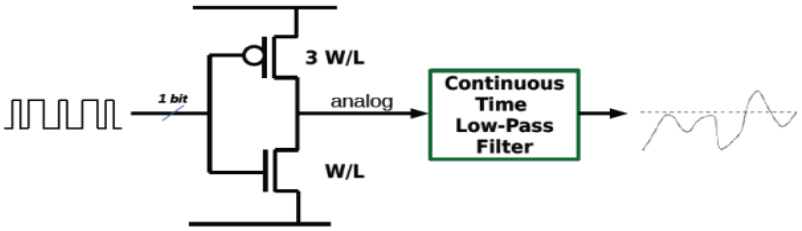
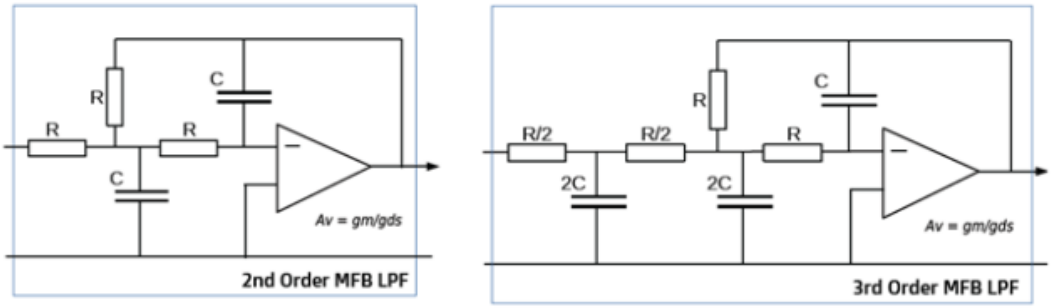


Figure 9. 1-bit DAC implemented with a CMOS inverter

Figure 10 illustrates the low-pass filter constructed using a 2nd or 3rd order multiple feedback analog continuous-time filter, commonly referred to as a Rauch filter [4]. The filters' bandwidths are set at 16kHz.



(a) (b)

Figure 10. 2nd (a) and 3rd (b) order low-pass continuous time Rauch filters

The spectrum of the DAC, including the 2nd or the 3rd order low-pass continuous filtering, is depicted in **Figure 11**. The sampling frequency is 16 MHz. It is worth noting that the CMOS inverter and the continuous time analog filter are modeled and simulated in the analog domain. The amplifier is modeled as a transconductance and a limited output conductance.

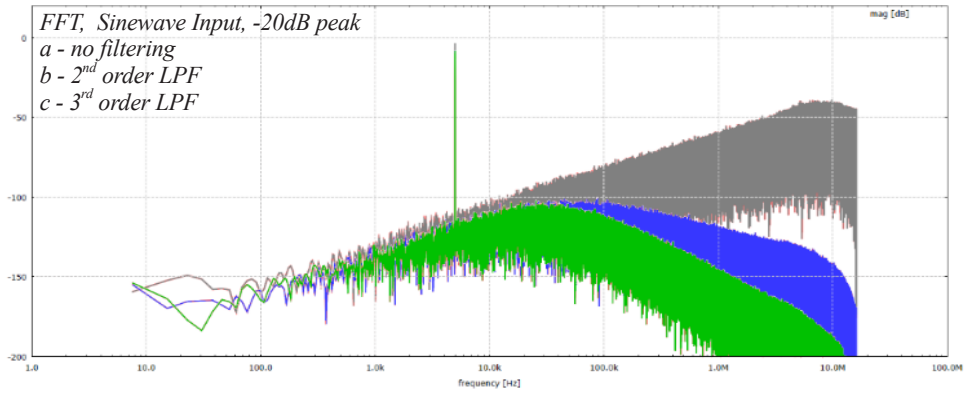


Figure 11. Output spectrum of the DAC (i.e. after the analog filtering)

A Total Signal-to-Noise Ratio (TSNR) is presented in **Figure 12**. An effective number of bits (ENOB) of 13 bits is achieved on a signal bandwidth of 16 kHz.

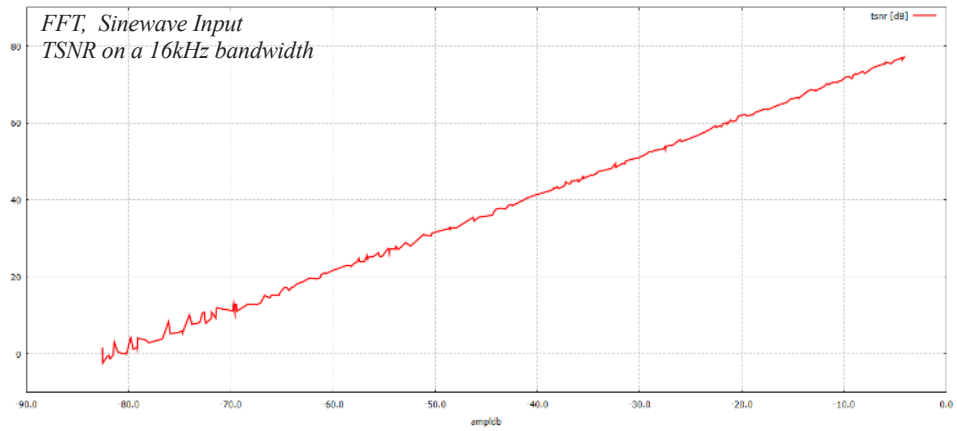


Figure 12. TSNR of the DAC, using a 5.0 kHz sinewave input

4. Conclusion

The proposed structure highlights four crucial features: prioritizing digital over analog for superior silicon efficiency in modern CMOS nanotechnologies, using a first-order sigma-delta modulator to streamline analog filtering, proactive elimination of deadly parasitic oscillations, and use of a simple CMOS inverter to convert the 1-bit output of the twin modulator. These features together guarantee minimal distortion, ensuring a high yield and trouble-free production.

Disclosure statement

The authors declare no conflict of interest.

References

[1] Candy JC, Temes GC, 1992, Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation, IEEE

Press, New York.

[2] Leduc Y, Mequin J, Jacquemod G, 2014, NAPA un Compilateur Construit Pour la Simulation Rapide de Systèmes Hétérogènes Présents ou Futurs, FETCH, Ottawa, Canada.

[3] Marsaglia G, 2003, Xorshift RNGs. Journal of Statistical Software, 8(14).

[4] Foster E, 1965, Active Low-Pass Filter Design. IEEE Transactions on Audio, 13(5).