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Design of Signal Lamp Filament Monitoring Alarm Instrument

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Abstract: To improve the reliability of the light emitting diode (LED) signal lamp filament current monitoring alarm instrument for metro systems, a new type of hot standby online monitoring apparatus was developed which is based on synchronous transmission data (STD) bus technology. In this system, a double hot standby mode can be achieved by adopting bus arbitration. In addition, to detect the effective value of alternating current which is from 0 to 200 mA in the signal lamp lighting circuit, a precision rectifier signal conditioning circuit and an isolated acquisition circuit were designed. This new type of alarm instrument has high detection accuracy and could meet the functional requirements for metro signal systems after comparing it with some industry products that were applied on the spot.

Keywords: Signal lamp; Monitoring alarm instrument; Precision rectifier signal conditioning circuit

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1. Introduction

Currently, the railway signal lamp filament alarm monitoring device is composed of several stand-alone acquisition boards. Each acquisition board is connected to the host computer through an RS-485 bus for online monitoring of the signal machine's working status. During daily use, the instrument may experience issues such as the crash or communication failure of a certain acquisition board. Additionally, the manual winding of the alternating current (AC) transformer in the sampling circuit of the acquisition board results in inconsistent parameters, making calibration inconvenient. Referring to relevant literature, it is found that although most of the monitoring and alarm methods in the literature require the installation of outdoor monitoring units and the use of controller area network (CAN) buses or power carrier methods to transmit monitoring data back, this approach uses a large number of cables, has high transformation costs, low economic efficiency, relatively complex structures, and issues such as low current detection accuracy, susceptibility to temperature and other factors, and frequent occurrences of crashes or even no alarms. With the rapid development of intelligent rail transit control systems, the requirements for the safety and fault tolerance performance of monitoring systems are becoming increasingly high. This article proposes the use of STD buses to design a dual-machine hot backup signal machine fault alarm instrument. This design does not require the installation of outdoor monitoring modules or outdoor cables, saving a significant

amount of engineering transformation costs. It can perform stable real-time online inspections of 72 channels of 0 to 200 mA AC small signals and check the display status of 72 signal lamp positions. It can cope with various harsh electromagnetic environments, temperature, and humidity conditions, making it a simple, low-cost, and highly reliable design solution [1–6].

2. General design

This system is mainly composed of Processor A board, Processor B board, N dynamic acquisition boards, N current acquisition boards, one communication board, and one power supply board. Information exchange between these boards is achieved through the STD bus.

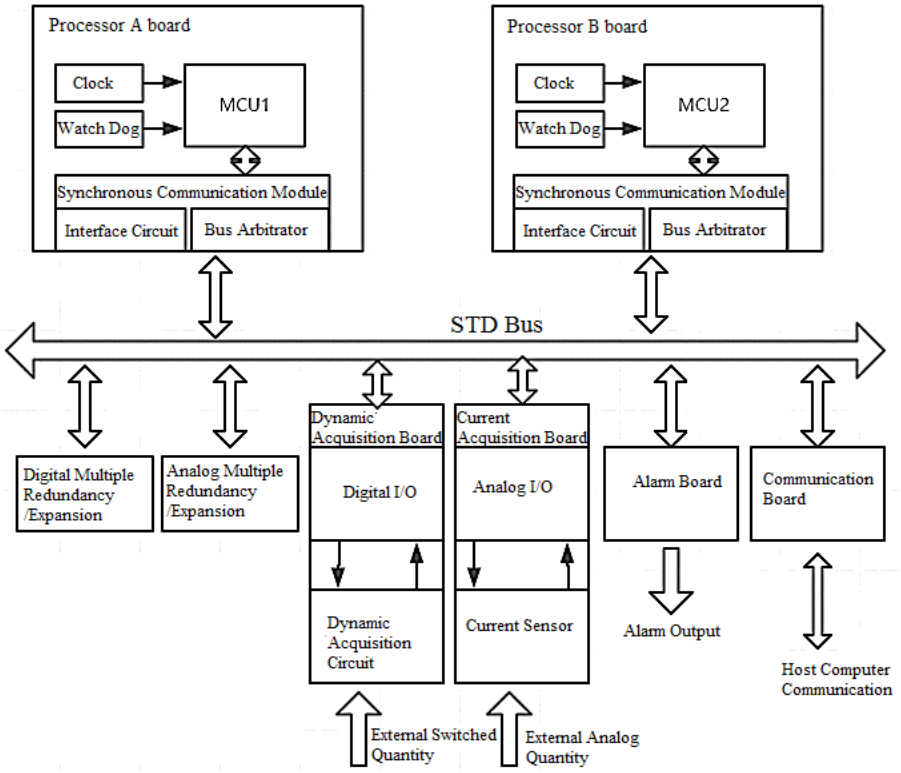

Figure 1. System structure diagram of LED railway signal lamp filament alarm monitoring device

Figure 2. Appearance diagram of LED railway signal lamp filament alarm monitoring device

The system structure diagram is shown in Figure 1. The Processor A board and Processor B board are responsible for cyclically reading the switching signals from each dynamic acquisition board and the analog-to-digital (AD) sampling values from each current acquisition board, and controlling the LED indicator status on the

front panel of the dynamic acquisition board. The dynamic acquisition board collects the lighting status of outdoor signal lamps, and there are small LED indicators on the panel to indicate the status of outdoor lighting points. The current acquisition board is used to collect the control loop current of each signal lamp's lighting disk. To avoid affecting the original signal control circuit, the system adopts current transformer isolation for sampling current. The alarm board is used to send alarm information to Processor A and B boards and emit alarm sounds. The communication board uses the FlexRay bus to communicate with the host computer, enabling real-time feedback on current alarm information, lamp status, and lighting data. The power supply adopts a dual-path hot standby switching power supply, with the main power path realized through a reverse excitation converter feedback circuit.

3. Implementation of key technologies for dual-machine hot backup

3.1. Design of dual-machine hot backup hardware structure

The core components of dual-machine hot backup consist of two identical processor boards, as shown in **Figure 3**. The processor board includes a PIC16F887 microcontroller, a bidirectional buffer for the data bus, a three-state buffer for the address bus, a reset circuit, random access memory (RAM), a clock source, and other components.

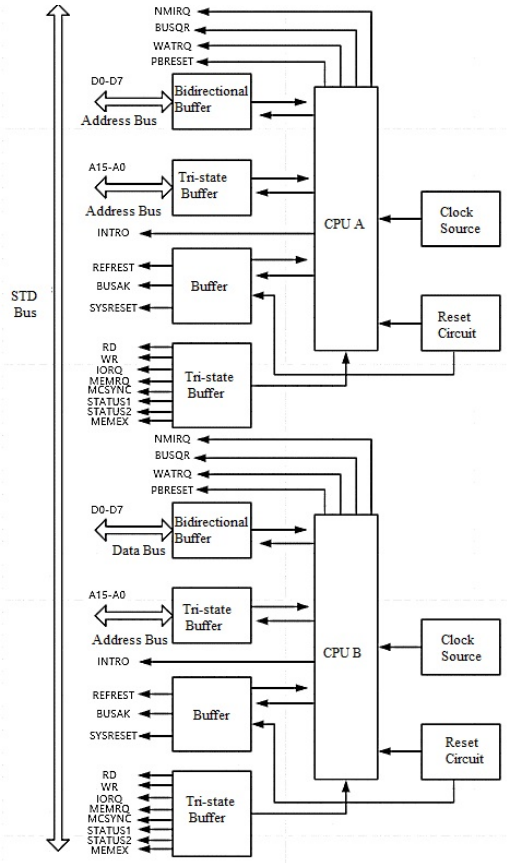

Figure 3. Simplified diagram of dual-machine hot backup processor structure based on STD bus

The important functional module of dual-machine hot backup—the arbiter—is shown in **Figure 4**. The hardware arbiter is a crucial circuit in this system, primarily used to allocate bus resources to the processors. The hardware arbiter determines the priority of processor access to the bus. By setting the corresponding priority chain inputs and outputs on the arbiter, it is possible to configure the access priority. Processors with higher priority are given preferential access to the bus, while other functional boards must wait until the bus control is released by the current board. Once the operational cycle is completed, the arbiter controlling the bus unlocks the STD bus for

other processors that have requested access[7-9].

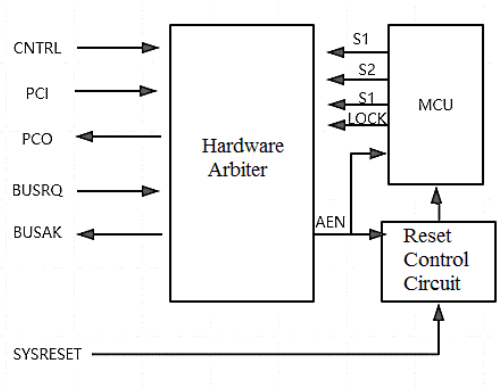

Figure 4. Simplified diagram of hardware arbiter structure

3.2. Selection of address bus and data bus circuits

The circuit diagram of the STD bus driver and buffer is shown in **Figure 5**. The system selects eight STD bus address lines (A0 to A7) and uses the driver chip 74LS245 as the address bus driver. The system employs an eight-bit data bus, controlled by the RD0-RD7 ports of the microcontroller, and utilizes the 74LS245 bidirectional data buffer as the data bus driver. Data read and write operations are controlled by the arbiter node enable (ANE) signal, which is issued by the arbiter. Only when the current processor board has priority can it perform read and write operations on the bus data.

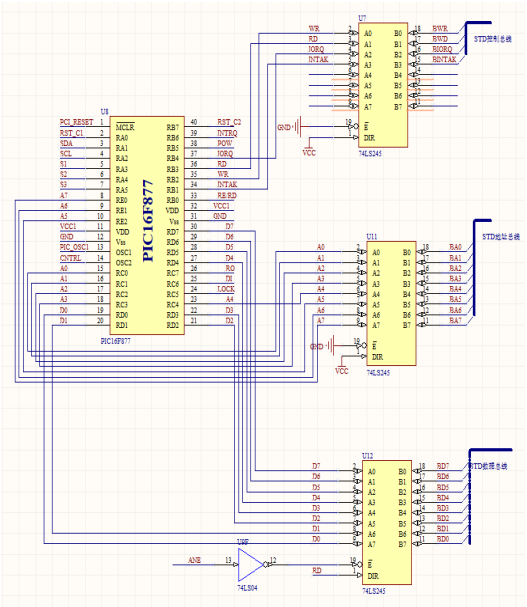

Figure 5. Design of STD bus interface circuit

3.3. Design of bus arbiter

The bus arbiter is designed using the complex programmable logic device (CPLD) chip GAL16V8D. As shown in **Figure 5**, the bus arbiter has six input terminals: S1, S2, S3, priority chain in (PCI), bus acknowledge (BUSAK), and bus request (BUSQR). The first five signal lines are used to receive bus communication requests and control priority requests from processor boards A and B to the arbiter. When S1, S2, and S3 output the “101” signal, it is considered a bus request signal. When they output the “011” signal, it indicates setting a high priority for the

output chain. When they output the “001” signal, it indicates setting a low priority for the output chain. PCI is the priority chain output signal terminal. BUSQR is used to receive bus requests, and BUSAK is used to receive bus responses.

The bus arbiter has four output terminals: BUSAK, BUSQR, PCO, and ANE. Among them, BUSAK is the bus response issued by the current master controller. BUSQR is the bus request issued by the currently unused device. After the master device receives it, the arbiter judges whether to release the bus based on priority. If the conditions are met, the bus is released and responded to through BUSAK. The standby machine receives the priority chain output (PCO) from the main board. ANE is the bus occupancy signal, informing the processor that it has obtained the current bus communication right.

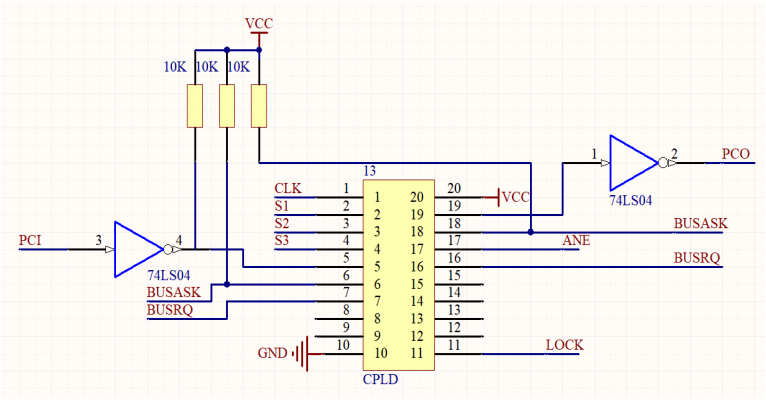

Figure 6. Design of STD bus interface circuit

The timing diagram for the request to use the bus between two bus arbiters is shown in **Figure 7**. The working process is as follows:

(1) Processor board A submits a bus request to arbiter A by issuing the “101” request signal.

(2) Arbiter A then submits a bus request to arbiter B.

(3) After confirming the PCI and PCO signals, arbiter B releases the bus control to arbiter A.

(4) Arbiter A acquires the control of the bus.

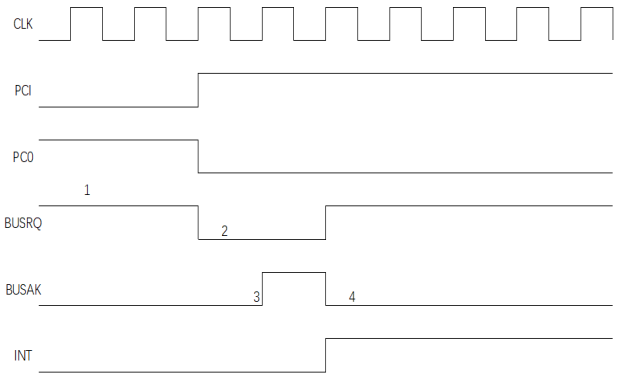

Figure 7. Timing diagram for bus request from arbiter A to arbiter B

4. Key technology implementation for AC effective value detection

The current acquisition unit consists of a signal conditioning module and a transformer and is ultimately collected by eight independent AD converters on the current acquisition board. In the subway signaling system, the normal

lighting current in the LED signal lighting circuit ranges from 100 mA to 150 mA AC, with a power supply voltage of 110 V AC or 220 V AC and a frequency of 50 Hz. Therefore, it is necessary to condition and shape the AC signal into a direct current (DC) signal for AD acquisition. Additionally, to ensure the safety of the original signaling system, the system uses an AC transformer to convert the current range from 0 mA to 200 mA, which is then sent to a precise rectification and conditioning circuit. The front stage of this circuit is an amplification circuit, and the rear stage is a precise rectification circuit that can shape small AC signals into nearly DC signals with very small ripples. **Figure 8** shows the schematic diagram of the high-precision rectification circuit of this system, and **Figure 9** shows the actual printed circuit board (PCB). Through Multisim simulation, it can be seen that the circuit has excellent conditioning and shaping effects, and has significant advantages in stability and accuracy compared to traditional capacitor integration circuits [10-15].

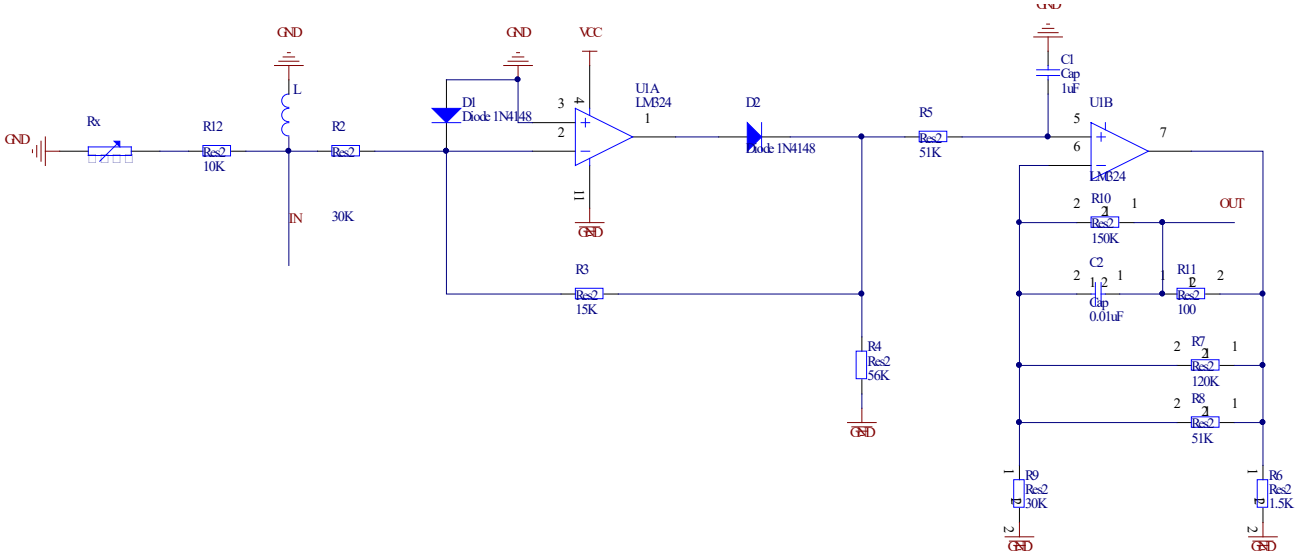

Figure 7. Schematic diagram of precision rectification and conditioning circuit for AC signal

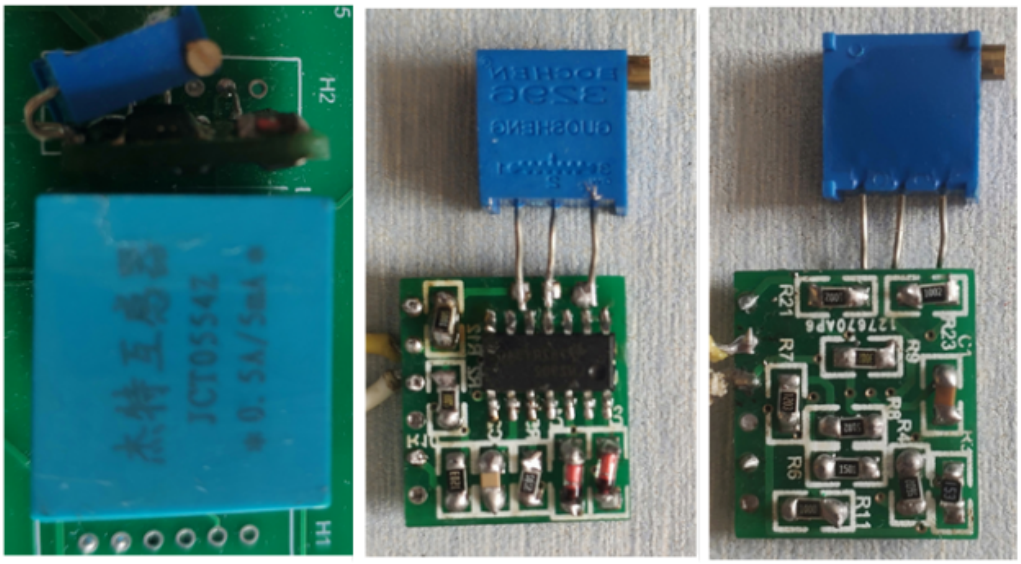

Figure 8. Precision rectification and conditioning circuit board for AC signal

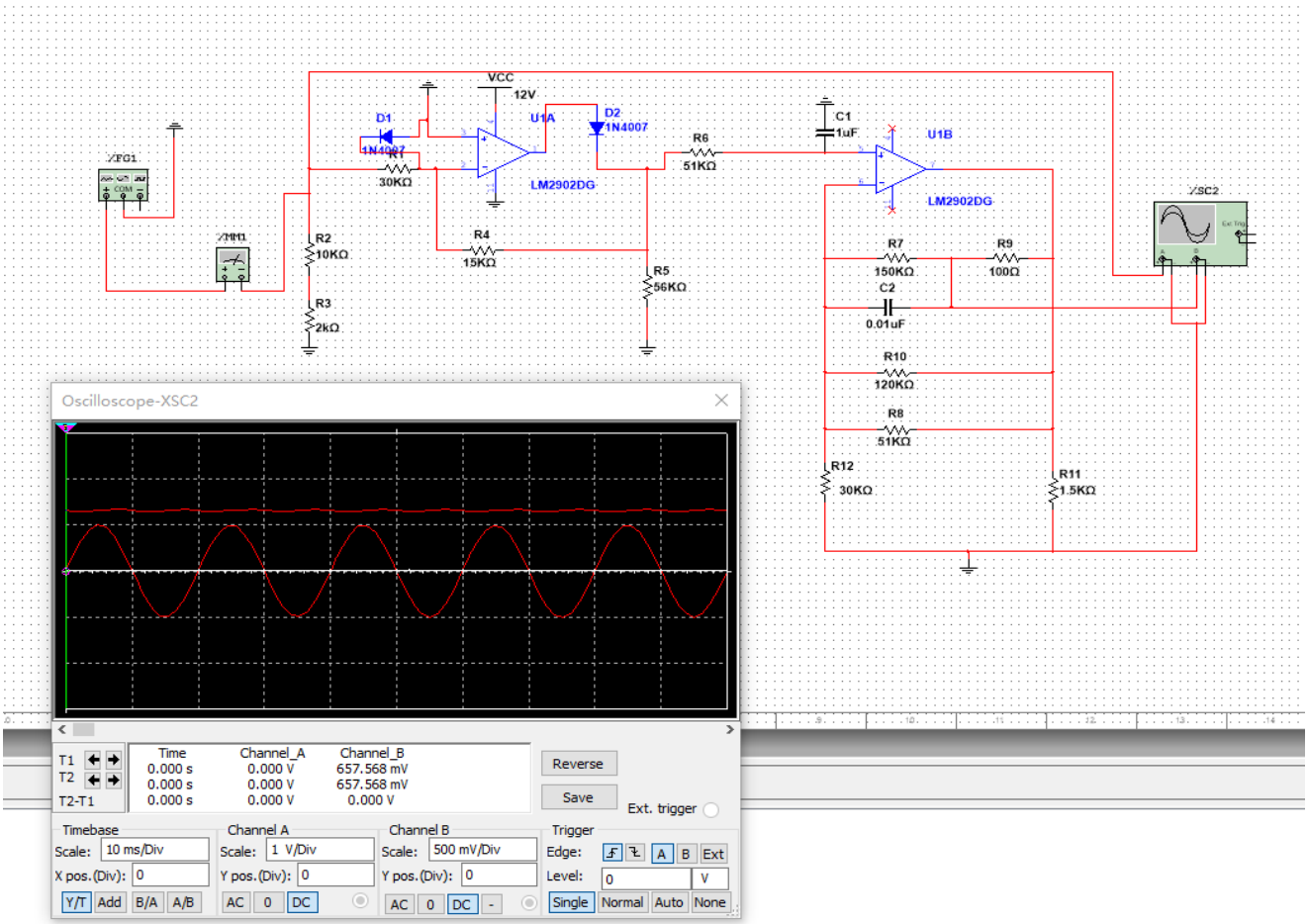

Figure 9. Multisim simulation diagram of precision rectification and signal conditioning circuit

5. Conclusion

The filament alarm monitoring device for railway signal equipment adopts the classic and highly reliable STD bus technology to design a dual-machine hot standby system that is simple, reliable, and does not require the installation of outdoor monitoring units, resulting in low retrofit costs. The designed precision rectification circuit achieves the conditioning and effective value collection of small AC signals without affecting the original lamp circuit, which has better consistency and stability compared to traditional precision rectification schemes. After laboratory testing and comparison with the XH-BJDW-72 LED signal equipment fault alarm instrument, the current collection accuracy is consistent. Compared to the traditional alarm instrument using RS485, it has better communication real-time performance and reliability of the FlexRay bus in terms of the number of acquisition channels. It can meet the needs of rail transit engineering in terms of functionality.

Disclosure statement

The author declares no conflict of interest.

References

[1] Luan Q, Ma Z, 2017, Design and Application of Real-time Monitoring and Alarm Device for High-speed Railway Signal Equipment. Railway Telecommunications & Signal, 53(08): 39–41.

[2] Liu H, Hu Y, 2017, Real-time Monitoring System Proposal for High-speed Railway Signal Equipment. China Science and Technology Information, 7: 85–86.

[3] Liu H, Hu Y, 2013, Analysis and Application Discussion of Centralized Monitoring of Signal Filament Circuit Current Information. Railway Communications and Signal Engineering Technology, 10(05): 56–57.

[4] Wuhan Railway Bureau Electric Service Department, 2015, Guide to Centralized Monitoring Information Analysis for Signals. China Railway Publishing House, Beijing.

[5] Zeng Y, 2011, Research on Detection Technology of Train Signal Circuit Current, thesis, Beijing Jiaotong University, 6: 20–25.

[6] Chen G, 2014, Research on Key Technologies of Safety Computer System and Safety Control Mechanism for Rail Transit, thesis, Doctoral Dissertation of Lanzhou Jiaotong University, 6: 28–40.

[7] Fang L, 2004, Implementation of High-Speed Communication on STD Bus for Multi-CPU Systems. Electronic Quality, 2004(08): 73–74.

[8] Ma R, 2000, Comparison of STD, CAMAC, and VXI Bus Technologies. Weapon System, 1: 45–49.

[9] Chen R, 1995, Development of High-Precision A/D Template for STD Bus Industrial Control Computer. Chemical Industry Automation and Instrumentation, 1995(01): 36–39.

[10] Yang J, Yang C, 2014, Railway Signal Lighting Device Based on Anti-Excitation Converter Feedback Circuit. Electronic Components, 37(05): 949–952.

[11] Wei Q, 2014, Fault-Tolerant Technology for Spacecraft Control Computers. National Defense Industry Press, 2014: 196–219.

[12] Liu S, Feng T, Chen Y, et al., 2016, Precision Rectification Circuit for High-Frequency Weak Signals Based on Current Mode. Modern Electronic Technology, 2016: 139–146.

[13] Zhang Y, Shi Q, 2017, Design of Isolated AC Differential Signal Conversion Equipment. Foreign Electronic Measurement Technology, 2017: 61–64.

[14] Wei L, Gao Q, 2023, Design of High-Precision Three-Channel Weak Signal Processing Circuit. Instrumentation Technology and Sensor, 2023: 52–55.

[15] Yang D, Hu J, 2021, Analysis of Precision Rectifier Circuit Simulation Model. Popular Electricity, 2021: 49–51.