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A Study on the Design Method of Hybrid MOSFET-CNTFET Based SRAM – A Secondary Publication

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Abstract: More than 10,000 carbon nanotube field-effect transistors (CNTFETs) have been successfully integrated into one semiconductor chip using conventional semiconductor design procedures and manufacturing processes. These transistors offer advantages such as high carrier mobility, large saturation velocity, low intrinsic capacitance, flexibility, and transparency. The three-dimensional multilayer structure of the CNTFET semiconductor chip, along with ongoing research in CNTFET manufacturing processes, increases the potential for creating a hybrid MOSFET-CNTFET semiconductor chip. This chip combines conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) and CNTFETs in one integrated system. This paper discusses a methodology to design 6T binary static random-access memory (SRAM) using a hybrid MOSFET-CNTFET. This paper introduces a method for designing a hybrid MOSFET-CNTFET SRAM by leveraging existing MOSFET SRAM or CNTFET SRAM design approaches. Additionally, this paper compares its performance with conventional MOSFET SRAM and CNTFET SRAM designs.

Keywords: MOSFET; CNTFET; SRAM; Hybrid; Carbon nanotube

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1. Introduction

For a long time, integrated circuits have increased the speed of circuits, lowered operating voltages, and improved integration by scaling down semiconductor device dimensions. However, as the channel length of metal-oxide-semiconductor field-effect transistors (MOSFETs) has decreased to the nanometer scale, additional improvements in MOSFET performance have become difficult due to short channel effects such as drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL), hot carrier effects, punch through, and leakage current. While the introduction of fin-shaped field-effect transistors (FinFETs) has helped alleviate some of these issues, there is ongoing demand in the market for continuous performance enhancement of semiconductor devices, driving interest in new materials and structures to further improve the performance of existing semiconductor devices [1-6].

Connecting the source and drain of conventional semiconductor devices with highly conductive carbon nanotubes (CNTs) has enhanced the performance of these devices, overcoming many known issues

and limitations, and positioning them as promising next-generation semiconductor devices. CNTs used in carbon nanotube field-effect transistors (CNTFETs) are broadly classified into semiconducting CNTs and metallic CNTs, with the need for techniques to extract only semiconducting CNTs to control the current in CNTFETs. Currently, techniques for extracting only semiconducting CNTs have achieved purity levels of up to 99.99%. Furthermore, the distribution of CNT diameters, which determines the threshold voltage distribution of CNTFETs, has been steadily decreasing, contributing to the realization of stable CNTFET circuit implementations. In addition, physical and chemical process improvements of CNTFETs or CNTs are expected to play a crucial role in enhancing the performance of CNTFETs and expanding their range of applications. These improvements will enhance parameters such as electron mobility, on/off ratio, operating frequency, power consumption, performance differences between N-channel FETs (N-FETs) and P-channel FETs (P-FETs), and substrate flexibility, thus improving the performance of CNTFETs and expanding their utility [1-12].

CNTFETs with these advantages have raised expectations for the mass production of semiconductor chips utilizing CNTFETs, using existing industrial standard design procedures and process technologies to integrate more than 10,000 CNTFETs on a single chip. Moreover, the manufactured CNTFET chip, as shown in **Figure 1**, is structured in a three-dimensional multilayer design using existing semiconductor processes, demonstrating the possibility of implementing MOSFETs on one layer and CNTFETs on another. This suggests the potential for manufacturing hybrid MOSFET-CNTFET chips using existing semiconductor processes. Additionally, while most CNTFETs have been fabricated by placing CNTs on a silicon wafer (**Figure 2a**) and stacking drain or source contacts on top, recently developed inkjet printing technologies, as depicted in **Figure 2b**, allow for precise placement of CNTs on structures similar to conventional MOSFETs, opening up various possibilities for manufacturing hybrid MOSFET-CNTFET chips [5,6,13,14].

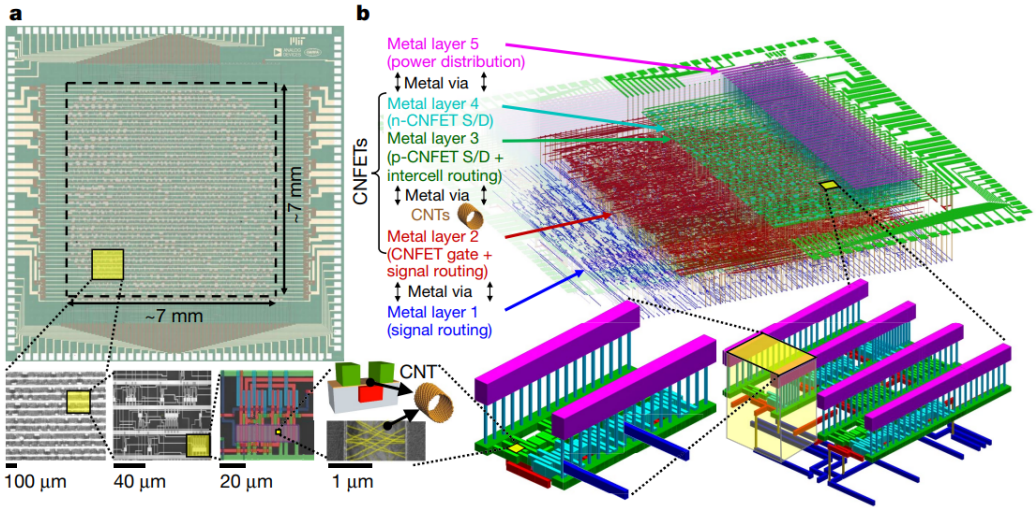

Figure 1. Microprocessor built from CNTFET [13]

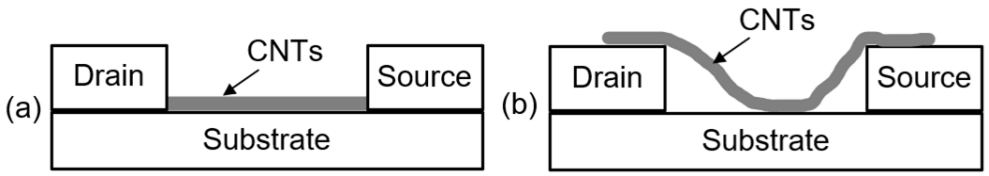

Figure 2. (a) Conventional deposition of CNTs [5]; **(b)** Deposition of CNTs by inkjet-printing [14]

In computer systems, static random-access memory (SRAM) is a crucial circuit block that needs to provide data for process operations at high speed. Typically, it occupies around 70% of the semiconductor chip area and is composed of SRAM cells that store minimal unit data such as 0 or 1, arranged in a repetitive pattern inside the chip. The performance of SRAM directly impacts the performance of microprocessors. Therefore, techniques to increase the speed of SRAM, reduce power consumption, and handle more data (ternary or quaternary) reliably have been continuously developed. Recently, various SRAM design studies utilizing CNTFETs have been underway [15-20].

Based on the current technological trends, the most realistic approach to implementing CNTFET chips at present involves designing circuit blocks as simple repetitive structures across the entire semiconductor chip. This reduces the impact of CNTFET process variations, allowing the implementation of circuit blocks with higher performance using CNTFET circuits compared to those implemented only with MOSFETs. In previous research [21], methods for designing SRAM with CNTFET were discussed, and their performance was compared with conventional MOSFET SRAM. This paper takes a step further by proposing a design method for hybrid SRAM, where complex data storage parts of SRAM cells are implemented with MOSFETs, and the data interconnection parts linking data storage and bit lines are composed of CNTFETs. The performance of the proposed hybrid MOSTFET-CNTFET SRAM will be compared with that of conventional MOSFET SRAM and CNTFET SRAM to assess the degree of performance improvement. For simulation verification, this paper utilizes the 32 nm PTM MOSFET library file and the Stanford 32 nm CNFET library file [22,23]. The aim is to discuss the design method for hybrid MOSFET-CNTFET SRAM using the existing design methods proposed in previous research for MOSFET SRAM or CNTFET SRAM and to compare their performance.

2. Hybrid MOSFET-CNTFET SRAM

This paper aims to discuss the design and performance enhancement of hybrid MOSFET-CNTFET SRAM based on the most fundamental SRAM cell known as the 6T SRAM cell. Referring to previous research results [21], it is referred to as hybrid SRAM for the sake of discussion efficiency. Hybrid SRAM, as shown in **Figure 3**, consists of a data storage section (MN3, MN4, MP5, and MP6) and a section (MN1 and MN2) connecting it to the bit lines (BL and BLB). This paper proposes a hybrid SRAM design that is less sensitive to process variations by constructing the relatively complex data storage section with MOSFETs, and the section connected to the bit lines with CNTFETs. In **Figure 3**, the transistors comprising the hybrid SRAM are represented using widely known conventional symbols for MOSFETs and include cylindrical symbols representing CNTs inside the CNTFETs to distinguish them from conventional MOSFET symbols. Furthermore, the channel of each transistor is depicted in grey for N-FETs and white for P-FETs.

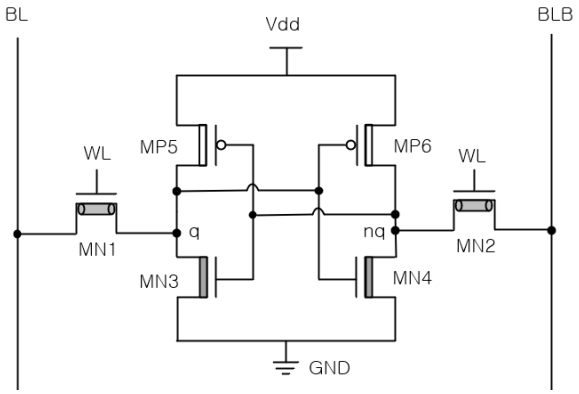

Figure 3. Hybrid MOSFET-CNTFET SRAM cell

To design the hybrid SRAM, it is necessary to determine the values of MN4/MN2 and MP5/MN1, similar to the conventional 6T SRAM design method. The “nq” value should be designed to be smaller than the threshold voltage of semiconductor devices to ensure that the stored data in the SRAM cell remains unchanged during reading. Since the data storage section in this paper is composed of MOSFETs, a threshold voltage of 0.18 V for MOSFETs was considered when considering the threshold voltage. The voltage value of “nq” according to MN4/MN2 is depicted in **Figure 4**, taking into account the CNT density of the CNTFETs when discussing each MN4/MN2. Specifically, CNT1 indicates that one CNT is placed within a 32 nm gate width, and CNT3 indicates that three CNTs are evenly spaced within the gate width. Similarly, the voltage value of “q” according to the ratio of MP5/MN1 and the CNT density is shown in **Figure 5**, and the “q” voltage value should be selected lower than the threshold voltage of MOSFETs to enable writing new data to the SRAM cell.

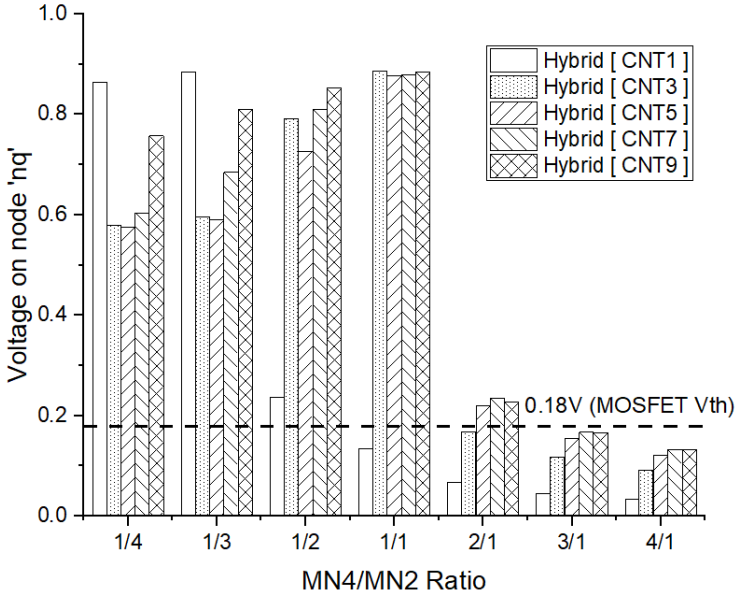

Figure 4. Voltage on node “nq” depending on MN4/MN2 ratio

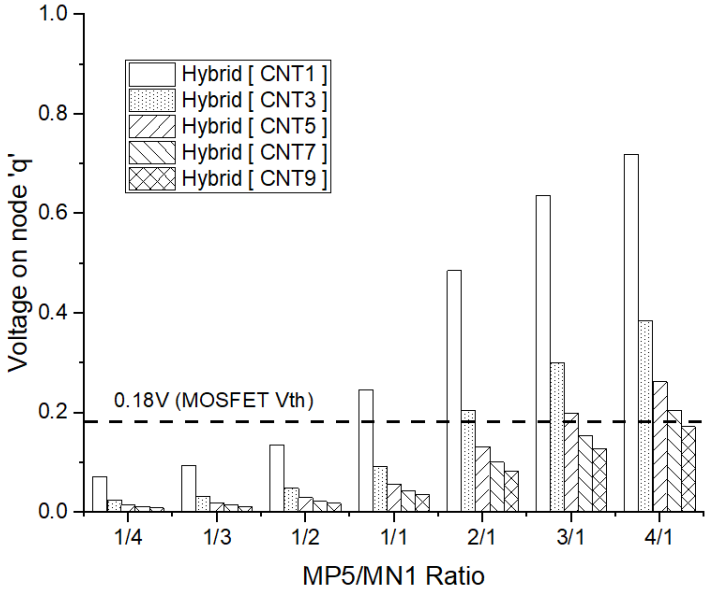

Figure 5. Voltage on node “q” depending on MP5/MN1 ratio

Through **Figures 4** and **5**, it was possible to use CNT7 and CNT9 when the ratios of MN4/MN2 and MP5/MN1 were 3/1, and only CNT9 could be used when the ratios were 4/1. In this paper, to minimize the area of the SRAM cell and reduce the possibility of process defects due to CNT arrangement, the ratios of MN4/MN2 and MP5/MN were selected as 3/1, and the CNT density was chosen as CNT7. Subsequently, the performance was compared with conventional SRAMs, i.e. all MOSFET SRAMs and all CNTFET SRAMs.

Table 1 shows the performance differences between all MOSFET SRAM, all CNTFET SRAM, and hybrid SRAM. In terms of read delay, hybrid SRAMs show performance comparable to all CNTFET SRAM and higher than all MOSFET SRAM. However, compared to all CNTFET SRAM, there is not much performance improvement, and instead, it consumes about 20 times more power. This indicates that CNTFETs can pass more current per unit area than MOSFETs, resulting in unnecessarily high current flow during read operations. This phenomenon can also be observed in the voltage characteristics of the "nq" node in **Figure 4**. In **Figure 4**, when MN4/MN2 is 1/4, 1/3, 1/2, and 1/1, it can be seen that if MN4 cannot pass enough current due to the significant current flow of MN2, the "nq" node does not decrease sufficiently in size to perform read operations easily. However, in write operations, such hybrid SRAM contributes to the performance enhancement of conventional SRAM. In write operations, all CNTFET SRAM does not show significantly better performance than all MOSFET SRAM and consumes more than twice the power. However, hybrid SRAM shows a delay reduction of more than three times compared to all MOSFET SRAM at similar power consumption. In other words, in terms of power delay product (PDP), all CNTFET SRAM improves read performance compared to all MOSFET SRAM but worsens write performance. However, hybrid SRAM overall enhances both read and write performance compared to all MOSFET SRAM. Therefore, unless high performance in read operations is crucial, it is unnecessary to manufacture SRAM with complex data storage sections using CNTFETs, even at the expense of higher process variation risks.

Table 1. Delay, power, and power delay product (PDP) of all MOSFET SRAM, all CNTFET SRAM, and hybrid SRAM

	Operation	CNT density	Delay (ps)	Power (μW)	PDP (aJ)
All MOSFET SRAM [23]	Read	N/A	234.90	0.041	9.54
	Write		35.58	0.604	21.48
All CNTFET SRAM [23]	Read	7	116.00	0.004	1.00
	Write		33.82	1.407	47.58
Hybrid SRAM	Read	7	104.00	0.080	8.31
	Write		11.70	0.752	8.80

3. Conclusion

In the era of the Internet of Things (IoT), the expectations for CNTFETs are steadily increasing, as they offer higher performance than conventional semiconductor devices, enabling not only data processing but also various applications in areas such as general-purpose sensors and wearable healthcare devices. Although mass production technologies for CNTFET-based semiconductor chips have not yet matured enough for commercialization, the utilization of CNTFETs even some circuit blocks of overall semiconductor chips could significantly enhance the feasibility of implementing CNTFET semiconductor chips. Therefore, this paper proposed a method for designing a hybrid SRAM composed of MOSFETs and CNTFETs, demonstrating that it achieves over three times faster write operations and twice the power improvement compared to SRAMs

composed solely of CNTFETs. This suggests a promising avenue for further exploration and advancement in the integration of CNTFETs into semiconductor chip designs.

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Disclosure statement

The author declares no conflict of interest.

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