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Research Article

PDN Tool: Ananalytical Model to Calculate the Input Impedance of Chip and Silicon Interposer Power Distribution Network

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Abstract:
This paper describes the job carried out for the developing of an analytical model that is able to calculates the input impedance of a power distribution network (PDN) by taking into account modeling of package and PCB. PDNs are usually already widely available, the work focuses on the chip and interposer PDN. The model has been used by an optimizer to determine the optimum position of the decoupling capacitors to be connected to the PDN.

0 Introduction

Nowdays the integration level of electronic devices built-in into the chips is extremely large. To meet the thermal requirements in terms of reliable design, it's necessary to reduce as much as possible the overall power demand inside the electronic components. To reach this goal, the voltage magnitude of signals are always being reduced. Consequently the combination of lower voltage swings and higher data rates , makes the signal integrity a very critical target to be satisfied in the designing of modern circuits. At the same time, due to the reduced range of the signal voltages for data transmission, also an efficient design of power distribution network (PDN) become a very important issue. If the power voltage isn't sufficiently clean and stable, the digital devices may not work properly. Usually decoupling capacitors (***decaps***) are inserted in the structure of PDN to minimize the ringing of the voltages rails. The effect of these capacitors is that of reducing the impedance of the PDN structure by providing additional and easily available charge storage to be delivered to the IC drivers.

The study of PDNs, recently become object of several academic research activities. This paper describes the work done to develop an equivalent circuit model that represents the PDN for modern integrated circuits. This model has been initially reported in [***Rif.1***] to realize an Optimizer that can evaluate the optimum positions of decaps in order to get the lowest profile for the PDN impedance in a given range of frequencies. The article is subdivided in five sections: the second one synthetically describe the structure of the device and of the PDN, the third section describes the method used for building the equivalent circuit. The fourth one shows how the model has been validated and the last section reports some conclusions.

1 Description of the Target System

The active portion of the system is constituted by two chips (chip1, chip2) interconnected between them by means of a silicon substrate named Interposer (Fig.1).

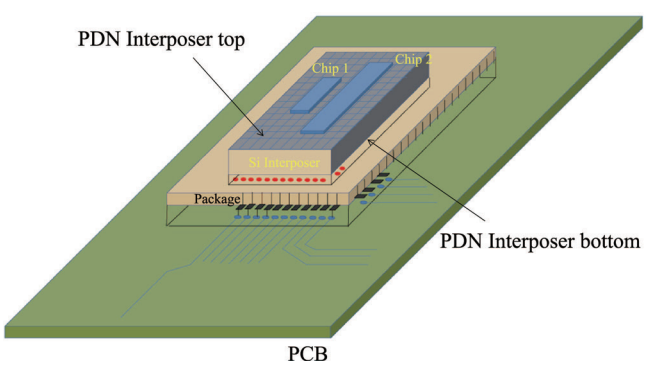

Fig.1 **Structure of the target system**

Then there is a package that makes the routing support for the connection to a printed circuit board (PCB).

The PDN of the chip is constructed with meshed power/ground cells as reported in Fig.2. The unit cell is modeled by a S-parameters network with four or five ports, specifically the fifth port is used for the connecting the decaps or the interposer bumps. The analytical derivation and assembly of the model of the unit cell is described in [***Rif.2***].

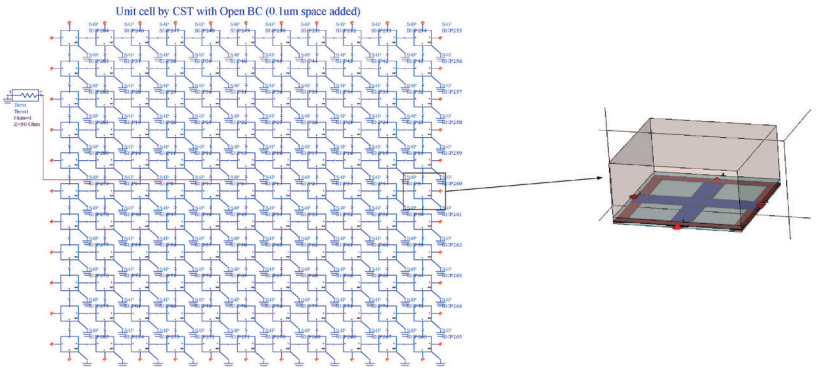

Fig.2 **Structure of the PDN**

There are two PDNs at both sides of Interposer, one in the upper edge and the other one in lower interposer side. Between these two PDNs a lot of trough silicon vias (TSV) are placed, to realize the power and the ground net connections and to accordingly reduce the TSV inductance as in Fig.3a,b.

The circuit model of the unit cell (UC) is showed in Fig.4

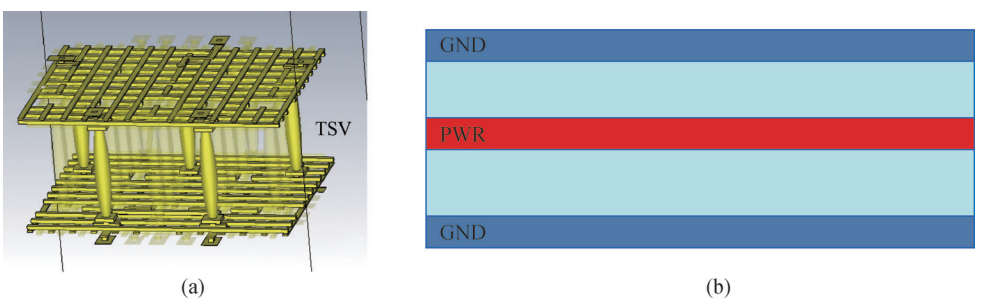

Fig.3 **Trough Silicon Vias TSV**

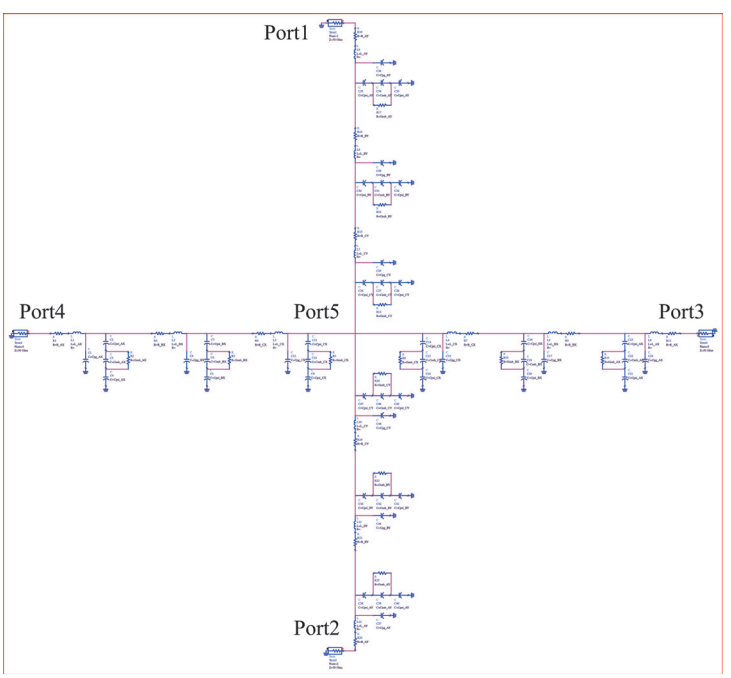

Fig.4 **Unit Cell**

Ports 1 through 4 are used to connect the UC with the surroundings to form the grid of PDN. The central port (or Port5), is used to connect: or the Chip to Interposer by means of the bump inductance, or the decap, or the TSV, or it is kept as output port for the connection to the I/O pin (drivers of the active circuit at chip level). Also unit cells with no central port are used to make the grid. UC 4 ports and UC 5 ports are alternated to reduce the dimensions of S-parameters matrices and so the complexity of the calculations. The overall structure of system is showed with some more details in Fig.5. In next Section 3, the analytical method used to calculate the S-parameters matrix of global system is described.

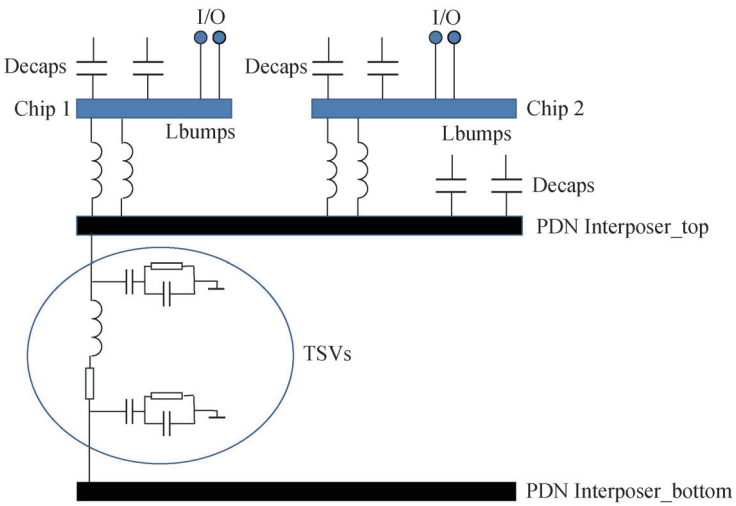

Fig.5 **Interconnections involved for the target system**

2 Analytical building of the Model

The model of the equivalent circuit for the global system showed in Fig.5 consists of the S-parameters matrix, ***Mgs***, whose order corresponds to the number of ports with which the global system will be interconnected to the external world. First the grid of unit cells is build by cascading the S-parameters matrices of unit cells by means of the function reported in [***Rif.3***]. The central ports that need for connecting the Chip1, Chip2, to Interposer through the Lbump inductance, the TSVs, the decaps and the I/O pins, all these ports remain in the resulting matrix ***Mgs***. The single models ***Ms*** are first and separately build for Chip1, Chip2, Interposer top, Interposer bottom. Then all these ***Ms*** matrices are cascaded together to get the total matrix: ***Mgs*** of the global system. To determine the optimum algorithm for building the grid of unit cells and so to calculate the ***Ms*** matrix for each component, an heuristic method was adopted. Many different strategies was developed: the first one consist of making grow up the ***Ms*** matrix by cascading one by one the unit cells to a temporary matrix ***Mr*** till to reach the final dimension (nxn) of ***Ms***. Another strategy was to build before the column of the grid and then cascading together that columns to obtain the final matrix. For each strategy the processing time was recorded. The algorithm selected was that one that had the lowest processing time. Synthetically it corresponds to build first the column of the grid, then ensemble together such columns and at each operation of assembly all the ports that aren't output ports are immediately eliminated from the *Ms* matrix. This shrewdness reduces the dimensions of matrices involved in the calculation, so reducing also the global assembly time.

Expressions used to connects the decaps are reported below:

The impedance matrix of the component is previously transposed in a way to bring all ports that must be connected to the decaps in the right lower section

$$(1)\quad \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

where V_2 is

(2) *being* Z_{cc} the diagonal matrix of capacitor impedances with:

$$(3)\quad Z_{cc} = \begin{bmatrix} Z_{C1} & 0 & 0 \\ 0 & Z_{Ci} & 0 \\ 0 & 0 & Z_{Cn} \end{bmatrix}$$

$$(4)\quad ZC_i = R_i + j\omega L_i + \frac{1}{j\omega L_i}$$

(5) where *Ri* and *Li* are the parasitic elements of decaps.

First, expression ***(5)*** is calculated, then the resulting matrix is transformed in S-parameters matrix and this last one is cascaded to the ***Ms*** matrix of the component (Chip1 or Chip2 or Interposer1). The final matrix ***Mcs*** included all the decaps.

In a similar but more simple ways, the Lbump inductance and the TSV equivalent circuits, are connected in the global system. For TSV, the equivalent circuit reported in [***Rif.4***] was adopted.

For connecting the TSV, first the parameters: Rt, Lt, CSiO2, CSi, RSi, with expressions reported in [***Rif.4***], are calculated. Then the ABCD matrix is generated, by means of the equations below:

(6) $Z_{pd} = 2R_{Si} + \left(\frac{1}{j\omega \frac{C_{Si}}{2}} \right)$

(7) $Z_p = \frac{Z_{pn}}{Z_{pd}}$

(8) $Z_p + \left(\frac{1}{j\omega \frac{C_{Sio2}}{4}} \right)$

(9) $Y_1 = \frac{1}{Z_1}$

(10) $Z_3 = 2R_t + j\omega(2L_t)$

(11) $Y_3 = \frac{1}{Z_3}$

(12) $Y_2 = Y_1$

(13) $A = 1 + \left(\frac{Y_2}{Y_3} \right)$

(14) $B = Z_3$

(15) $D = 1 + \left(\frac{Y_1}{Y_3} \right)$

The ABCD matrix so obtained is then converted to the S parameters matrix: S_{tsv}. This last one is then cascaded by appropriately connecting the ports, to the ***Ms*** matrix of Interposer2.

The connection for the inductances L_{bump} isn't detailed here.

An example of model used to do simulations and evaluate the results is reported in Fig.6

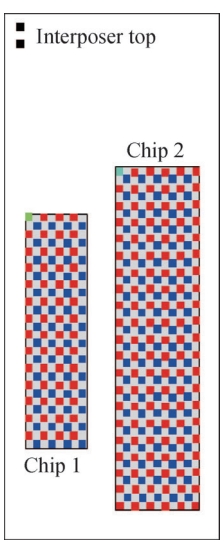

Fig.6 **Model example**

The test case used in Fig.6 is constituted by:

Interposer top PDN: 67x28 UCs
Chip 1 PDN: 30x8 UCs
Chip 2 PDN: 41x11 UCs
(UC => unit cell)

- UC with 5 ports for decap and I/O connection, Chip 1 offset (29;5)
- UC with 5 ports for decap and I/O connection, Chip 2 offset (23;15)
- UCs with 5 ports for decap and I/O connection (60+126=186 ports)
- UCs with 5 ports for connection to Interposer (60+100=160 ports)
- UCs with 5 ports, 4 external ports for case example
- UCs with 4 ports

For each component, the grid of cells is numbered as rows and columns and the origin is always the upper left corner

The offset above reported, indicates the number of row and column where is positioned the origin of Chip1, Chip2, with respect to the origin of the Interposer, top.

For simulations the ports considered as external or output (and so reported in the matrix ***Mgs***), of the global system are showed in Fig.7.

3 Validation of the Model

The "UAq PDN tool" was developed and in addition to the arguments that describe the structure of the system like number of rows and columns of the components, the assembly function also required the coordinates for the decap placement. As already previously said in the

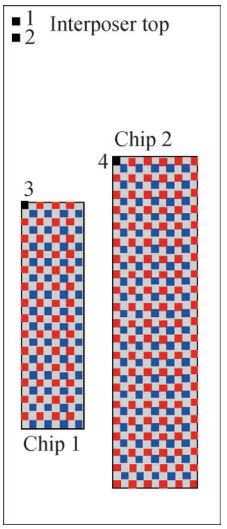

***Fig.7* Model example ports**

The input impedances are calculated for the ports 1,2,3,4,Z_{11},Z_{22},Z_{33},Z_{44}in the frequency range 10 MHZ, 40GHZ.

Results are reported in Figg.8.
The behavior of impedance is capacitive at "low" frequency while is inductive at more higher frequencies, about at 1 GHz.

Additional test cases were analyzed to verify the correctness of the developed models and to see the impact of decaps and Lbumps inductances in the structure.

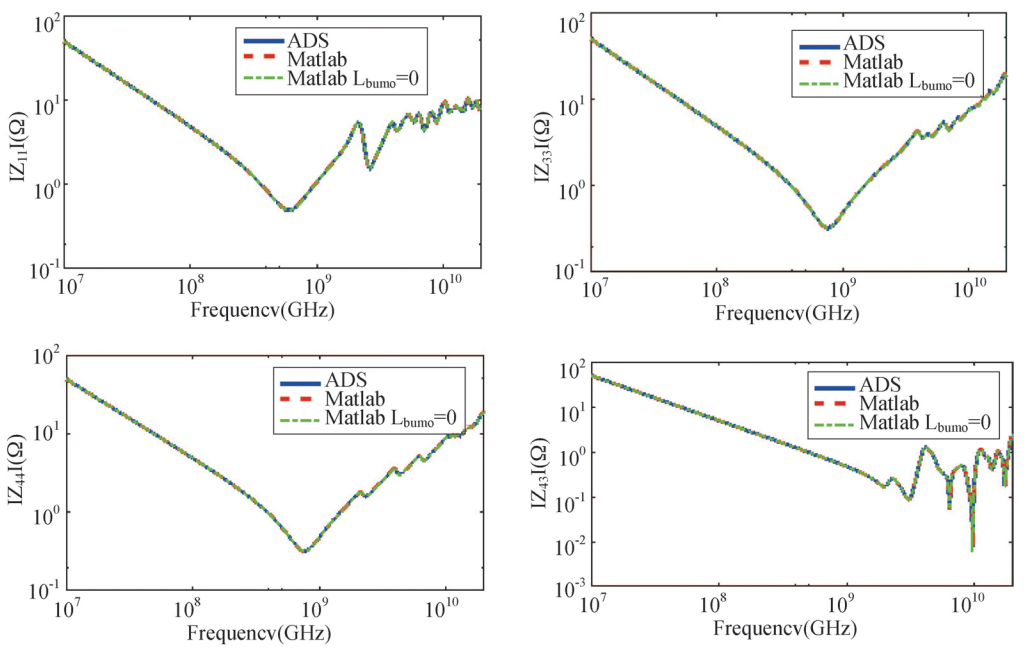

Fig.8 **Input impedances for the model described in Fig.6. Comparison with ADS simulations**

Introduction, this tool is used by an Optimizer that can indicate the optimum positions of decaps in order to get the lowest profile for the PDN impedance in a given range of frequencies. Such optimizer passes to the UAq PDN tool an initial position for the decaps by means of vectors of coordinates *X*,*Y*. The Matlab function calculates the input impedance at the ports of interest and returns these results to the optimizer. This last one checks if the currently impedance profile is lower with respect to a target, if a positive response is obtained, then the iteration is concluded, otherwise optimizer changes the values of *X*,*Y* and calls again the UAq PDN Tool.

For validating the model, the Keysight ADS commercial simulator was used. A circuit diagram representing the grid of PDN was designed by hand using the schematic editor of ADS. The multiport S-parameters block was used to load and assembly each portion of the PDN, from the single UCs to the overall PDN structure. A simplified example of circuit diagram is showed in Fig.9

Several test cases were analyzed in order to run a sufficiently large validation. The results obtained with

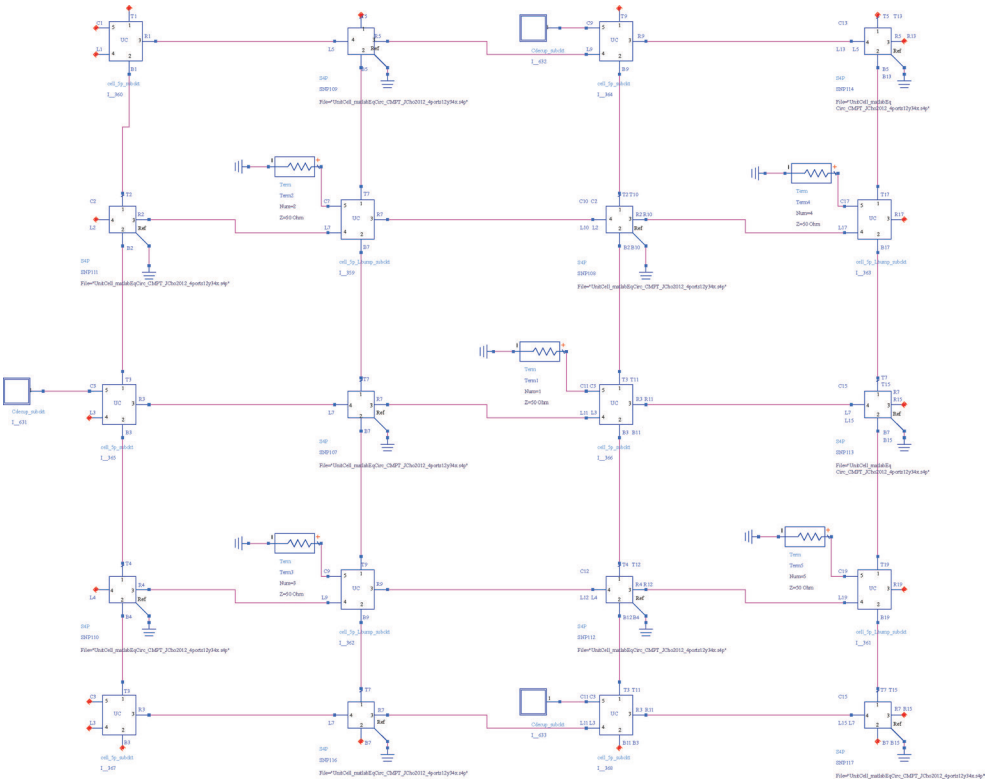

***Fig9*. Example of circuit diagram in ADS simulator**

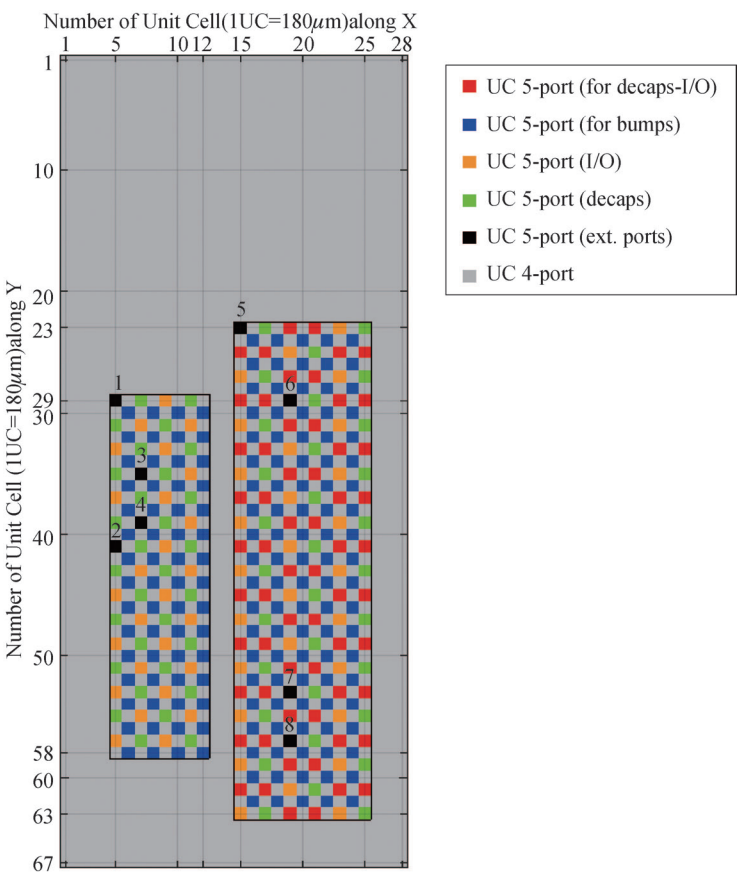

***Fig10.* Target System for Model validation**

Interposer top PDN: 67x28 UCs
Chip 1 PDN: 30x8 UCs
Chip 2 PDN: 41x11 UCs
Decap value = 1.16 nF,
ESR=10mΩ
Examples for the vectors of coordinates, for a simplified configuration, are reported below:
X_g=[1 3 3 3 3 3 3 4 4 6 6 8 8 10 10 12 12]
X_g=[3 1 5 1 5 9 13 2 4 2 4 2 4 2 4]
The vector Xg represents the number of column and Yg represents the number of row where is connected the decap: Ci. To the assembly function also the number of decap for each component is passed. In the above example we have: N_decap_Chip1=3; N_decap_Chip2=4; N_decap_Interposer1=10. So the first 3 positions of vector X_g, represent the coordinates of decap for Chip1 and so on.
The results are showed in Fig.11

the UAq PDN Tool were compared with simulations done with ADS. An excellent matching has always been found (see previous Fig.8).

Fig 10 is reports a target system where the effect of the connection of decaps and the variation in the L_{bump} values, on the PDN impedances is analyzed. The aim always is to augment the coverage and the confidence for the model validation.

It's also possible to do a comment about results reported in above Fig.11. There is a large impact of chip decaps on input and transfer impedances, while there are negligible differences when L_{bump}=2.9 pH is considered even up to 40 GHz.

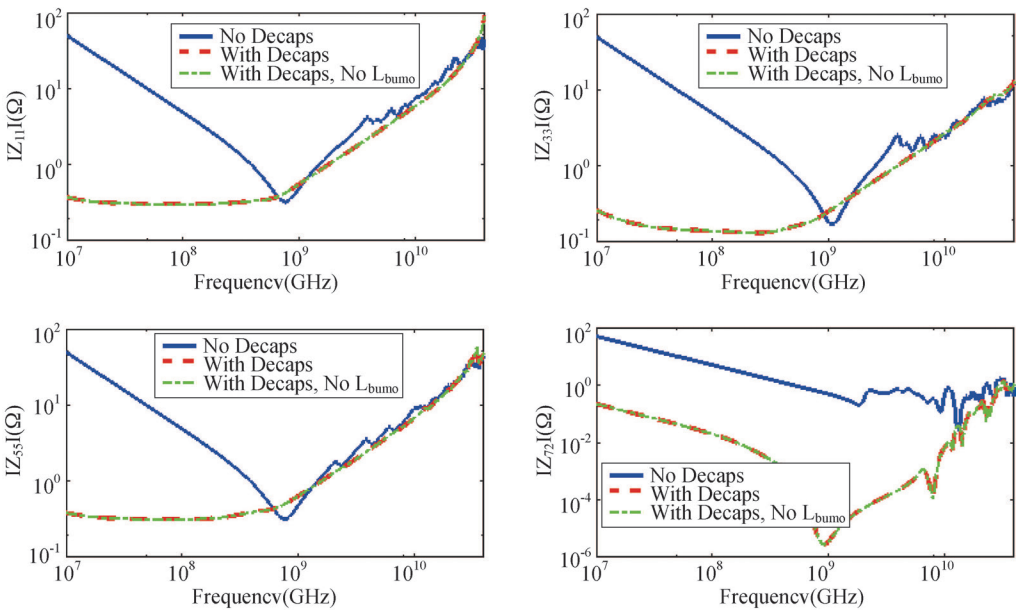

Fig11. **Effects of the connection of decaps and inductances Lbump for PDN impedance**

4 Conclusion

This work has showed how the effects of the PDN impedance is very important in the designing of modern and very complex electronic devices.

An accurate analysis of the PDN structure and the connections of decaps in such structure can significantly improve the impedance profile in a given range of frequency.

Different systems configurations are simulated up to 40 GHz to validate the model developed with the UAq PDN tool. The matching of results obtained with a commercial simulator and those obtained by the UAq PDN Tool was always excellent.

Having a lower impedance profile for the power voltages means to have more clean signals so granting the correct operating conditions of digital systems.

Acknowledgments

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