Journal of Electronic Research and Application

OPEN

EMI Reduction in Low Input Ripple DC-DC Converter using Chaos PWM technique

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Abstract: This paper presents a chaotic PWM switching technique for a high boost DC-DC converter with a very low ripple at the input current. The use of a choatic PWM allows a reduction of Electromagnetic In (EMI) at the output of power converters by spreading the energy spectrum of the output voltage. In this paper a chaotic PWM, using the Chua oscillator, has been implemented in Matlab for the converter under study and a comparison with a traditional PWM control has been done. A detailed description of the generation of the chaotic carrier is presented and the effect on the output EMI mitigation has been shown.

Key words: EMI; Chaotic PWM; Spreading Spectrum; DC-DC converter

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Introduction

The electronic power converters, used in many technology fields, such us automotive, renewable energy, aerospace, etc, are sources of Electromagnetic Interference (EMI) that can cause malfunctions in the electric/electronic devices that share the same electromagnetic environment of the power converters. The switching operation generates high du/dt and di/dt that can cause both conducted and radiated EMI[1]-[4].

For these reasons and in order to comply the limits imposed by the Electromagnetic Compatibility (EMC) standards, EMI reduction techniques have to be adopted; these are passive/active filters, shielding, optimization of layout, random switching techniques[5]-[10].

The use of filters, shielding and techniques of layout optimization have some drawbacks in terms of weight, volume and cost. Among the reduction methods, the random-switching techniques have been applied in the last decade, resulting the least-cost and effective solutions[11]-[15].

The main idea of these switching techniques is to spread the spectrum of the disturbances such that the power at specific frequencies is reduced to conform the EMI standards without any additional filters. Among these, the chaos technique is employed to switch the converter with chaotic PWM pulses obtaining a spreading of the output disturbances and a reduction of EMI[15]-[18].

A chaotic carrier waveform can be generated by digital or analog circuit[19]-[20]. The digital chaotic carrier is more accurate than the analogue one and the modification of its frequency and amplitude is simple by using a digital processor. On the other way, the cost of the digital implementation is higher than analogue one. In the analogue implementation, the chaotic frequency can be modified changing the resistance and the capacitance of the chaotic circuit. Due to the non-ideal characteristics of these passive components, the analog chaos carrier waveform is less accurate than digital one and the hardware implementation is more complex.

This paper proposes a chaos PWM switching technique for a high boost low input ripple DC-DC converter designed by the Authors[21]. The chaos carrier has been generated employing an analog circuit. In particular, among the chaotic oscillator existing in literature, the Chua's oscillator has been adopted[22]. This is a simple circuit that uses only two operational amplifiers that can be easily integrated on a chip. The performance of the DC-DC converter with a Chaotic PWM has been analysed and compared with the performance related to a traditional PWM. In particular, the spreading of the output voltage spectrum has been

verified and simulations have been done, using a high frequency (HF) model of the DC- DC converter under study, to validate the effects of the chaotic carrier to reduce EMI.

1 DC-DC Converter under Study

The low input current ripple high boost converter under study is shown in fig. 1. It is a current-fed step-up converter designed to produce an output voltage about four times higher than the input voltage and a low input current ripple. In Continuous Conduction Mode of operation, the state space equations of the converter in ON-state and OFF-state are, respectively:

$$\begin{cases} V_d - L_1\dot{x_1} - R_{L1}x_1 = 0 \\ L_2\dot{x_2} + R_{L2}x_2 - R_{C2}C_2\dot{x_4} - x_4 = 0 \\ x_4 + R_{C2}C_2\dot{x_4} + x_3 + R_{C1}C_1\dot{x_3} + RC_1\dot{x_3} = 0 \\ C_1\dot{x_3} = C_2\dot{x_4} + x_2 \end{cases} \quad (1.a)$$

$$\begin{cases} -V_d + L_1\dot{x_1} + R_{L1}x_1 + R_{C2}C_2\dot{x_4} + x_4 = 0 \\ L_2\dot{x_2} + R_{L2}x_2 + R_{C1}C_1\dot{x_3} + x_3 = 0 \\ -x_4 - R_{C2}C_2\dot{x_4} - x_3 - R_{C1}C_1\dot{x_3} + Ri_o = 0 \\ i_o = x_2 - C_1\dot{x_3} \\ C_1\dot{x_3} = C_2\dot{x_4} + x_2 - x_1 \end{cases} \quad (1.b)$$

where x is the state vector: $x = [i_{L1}\ i_{L2}\ v_{C1}\ v_{c2}] = [x_1\ x_2\ x_3\ x_4]$.
The state space averaging state equations are:

$$\begin{cases} \dot{x} = Ax + Bv_d \\ v_o = Cx \end{cases} \quad (2)$$

with $A = A_1D + A_2(1-D)$, $B = B_1D + B_2(1-D)$, and $C = C_1D + C_2(1-D)$; Vo is the output voltage, vd is the input voltage and D is the duty cycle[21].
The input ripple current mitigation, introduced by the converter, is shown in Table 1, that shows the comparison of the ripple generated by this DC-DC converter with the one generated by conventional boost topology.

2 Chaotic PWM Generation

The analogue chaotic PWM, used to switch the DC-DC converter under study, has been generated using the Chua's circuit. The analogue chaotic PWM signal is generated comparing the reference signal with a chaotic triangular carrier, as shown in Figure 2.
Figure 3. shows the chaotic generator. The chaotic triangular carrier, vc, is obtained by charging and discharging a capacitor, C6, by using a chaotic signal vchaos generated by a chaotic oscillator. The chaotic triangular carrier is generated between a lower limit Vlow, defined by the resistor R1 and R2, and a upper limit Vupp that is the sum of Vu, defined by R3 and R4, and of vchaos[22]. When vc is zero, at the start of the devices, or vc< Vlow< Vupp, the input of the R-S flip-flop are R=1 and S=0 that gives an output Qn+1=1. In this condition the switch S7 is ON and the capacitor C6 is charged by VCC. When Vlow < vc < Vupp, R=1 and S=1 and Qn+1=Qn, in this case S7 remains ON until vc reaches Vupp. When R=0 and S=1, Qn+1=0, S7 switches off and the capacitor C6 starts to discharge until vc reaches Vlow. Then, another cycle starts.
The chaotic behavior of Vupp, due to vchaos, makes chaotic vc, with a frequency fn=1/Tn. that varies chaotically around the converter reference frequency, fsw.
Among the well know chaotic oscillators, i.e. Chua's, Lorentz's and Chen's oscillators, in this work the Chua's oscillator is used to generate vchaos voltage.

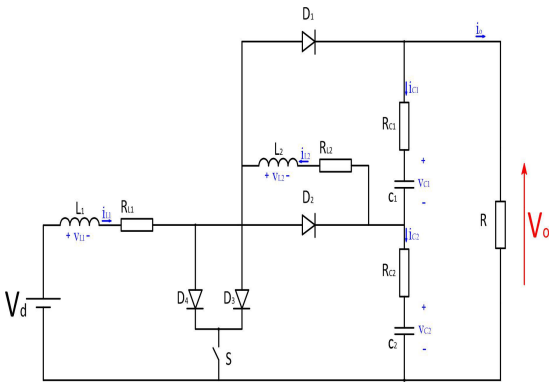

Fig.1 Low Current Ripple Step-up Converter

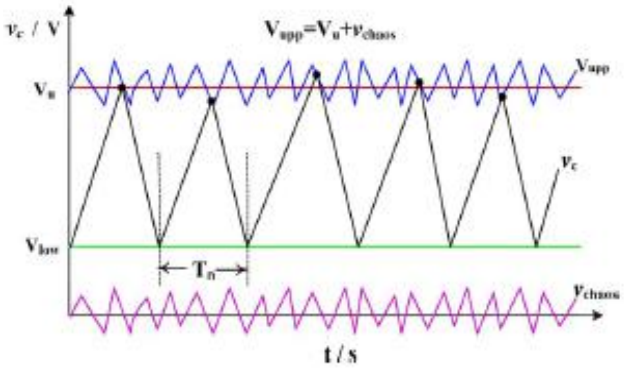

Fig.2 Chaotic Triangular Carrier

Table 1 Comparison with the Ripple of a Traditional Boost

Ripple i_{L1}%					
Vo	Boost	Low Ripple Boost	Vo	Boost	Low Ripple Boost
60	2.41	0.92	100	2.90	1.41
80	2.7	1.22	120	3.02	1.53

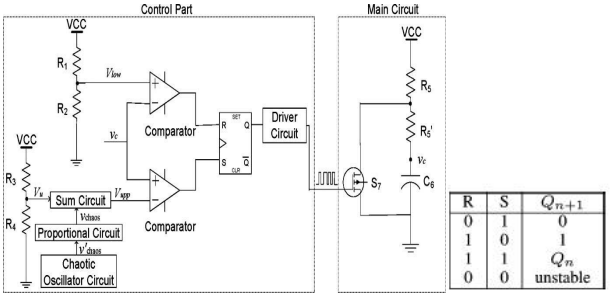

Fig.3 Generator of the Chaotic Triangular Carrier

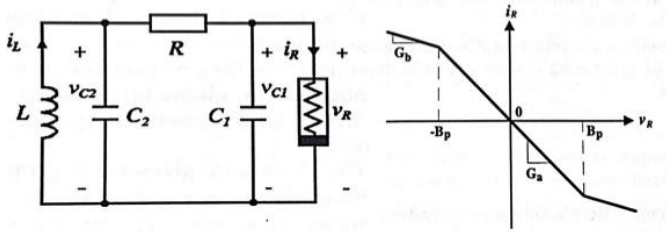

Fig.4 Chua's Circuit and *v-i* Characteristic of the Non Linear Resistor

Figure 4. shows a scheme of the Chua's oscillator. The dynamics of the Chua's circuit is described by the following equations:

$$\begin{cases} \frac{dv_{C1}}{dt} = \frac{1}{RC_1}(v_{C2} - v_{C1}) - \frac{1}{C_1}f(v_{C1}) \\ \frac{dv_{C2}}{dt} = \frac{1}{RC_2}(v_{C1} - v_{C2}) + \frac{1}{C_2}i_L \\ \frac{di_L}{dt} = -\frac{1}{L}v_{C2} \end{cases} \quad (3)$$

where:

$$f(v\_C1) = G_b v_{C1} + \frac{1}{2}(G_a - G_b)(|v_{C1} + B_p| - |v_{C1} - B_p|) \quad (4)$$

is the vR-iR characteristic of the non-linear resistor of the Chua's circuit. Chua's circuit is a very simple autonomous system that exhibits the complex behavior of bifurcation and chaos. The values of the parameter of the Chua's circuit define the value of the chaotic frequency fn of vchaos. The PWM chaotic signal to switch the DC-DC converter has been implemented in Simulink toolbox of Matlab. The Chua's circuit of Figure 4 has been implemented using the differential equation (3) with: R= 1800 , C1=10nF, C2=100nF, L=18nH.

The non-linear resistor defined by relation (3) has been defined by the following values: E=1,17V, Ga=-757, 57 S and Gb=-409,09 S. Wit these values a chaotic frequency, fn that varies chaotically around a reference frequency, fR=10kHz has been obtained. Figs. 5-7 show the obtained chaotic behavior of the waveforms generated by the simulated Chua's circuit. Fig. 8 shows the simulated chaotic carrier voltage, together with the generated Vupp and vchaos. The figure shows that a chaotic frequency around 10 kHz is obtained.

The behavior of the DC-DC converter has been studied using a classic PWM gate signal at a frequency of 10kHz and using the described chaotic PWM gate signal. The effect on the reduction of the harmonics amplitude of the converter output voltage has been studied and the mitigation effects on the output EMI have been verified.

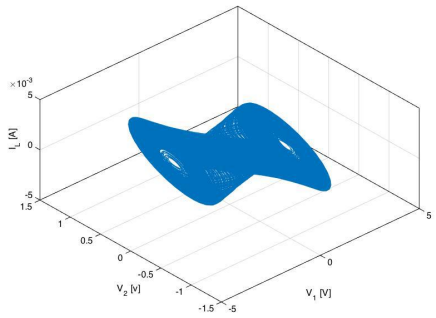

Fig.5 Simulated Chua's Circuit Waveforms

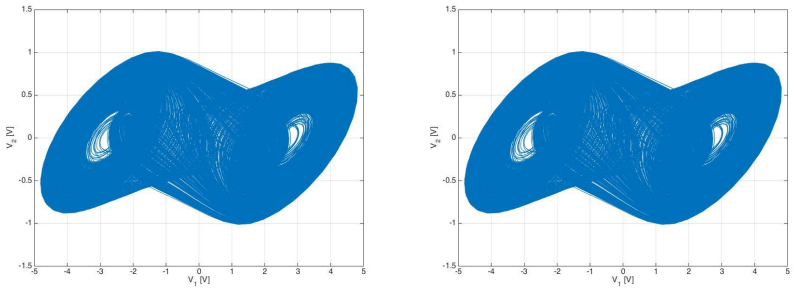

Fig.6 Simulated V2 vs V1 Chua's Circuit Voltages

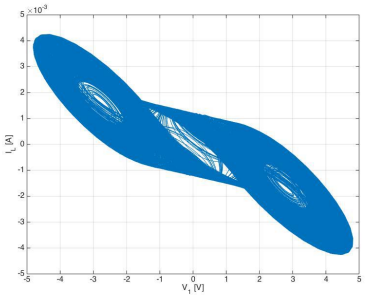

Fig.7 Simulated IL vs V1 Chua's Circuit Voltages

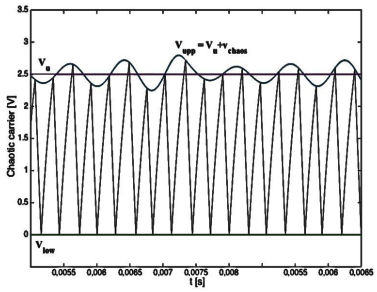

Fig.8 Simulated Chaotic Carrier Waveform

3 Simulations and Analisys of the Results

The effects of a chaotic PWM on reducing EMI at the output of the DC-DC converter under study have been studied and verified by Simulation analysis. Tests have been performed by using the Simulink-Matlab software platform, where the DC-DC converter has been modeled, together with the chaotic PWM signal.

The advantageous effects of a chaotic PWM are shown in Figure 9. where the Fast Fourier Transform of the output voltage with a classic PWM is compared with the FFT of the output voltage obtained using a Chaotic PWM. Figure 9. shows that a reduction of the harmonic amplitudes is obtained by a spreading the energy spectrum of the output voltage.

As a consequence of the results shown in Figure 9, a reduction of the output EMI of the converter is expected. To verify this effect, a High Frequency (HF) model of the DC-DC converter under study has been developed and the EMI using a chaotic PWM have been simulated and compared with that obtained using a classical PWM switching signal.

Figure 10. shows the developed HF model of the converter under study. The parasitic inductances of the cable, Lw, the stray capacitances to ground, Cg, of the converter are taken into account[4]. Moreover the HF models of the converter output capacitors have been developed[10]. The possible values of the considered parasitic elements for the converter under study are shown in Table 2.

Figure 11. shows the comparison of output EMI of the converter when a classic PWM and chaotic PWM switching signal is used. The Figure reports also the EMI limits defined by the EN 61800 standard. As the figure shows, with a chaotic PWM a reduction of about 20 dBV is obtained and this effect guarantees, also, the respect of the EMI standard limits.

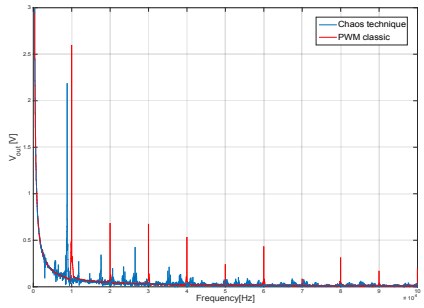

Fig.9 Comparison of FFT of Vout with Classic Chaotic PWM

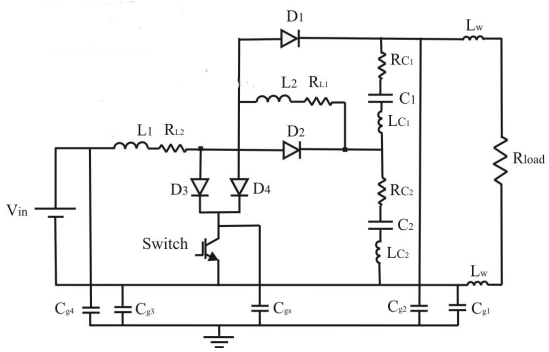

Fig.10 HF Model of the DC-DC Converter with Parasitic Parameters

Table 2 Possible Values of the Considered Parasitic Elements for the Converter

Parameters	Values	Parameters	Values
C_{g1}, C_{g2}	40 pF	R_{L1}	0.4Ω
C_{g3}, C_{g4}	30 pF	R_{L2}	0.8Ω
C_{gs}	40 pF	R_{c1}, R_{C2}	0.1Ω
L_w	30 pF	L_{C1}, L_{C2}	30nH

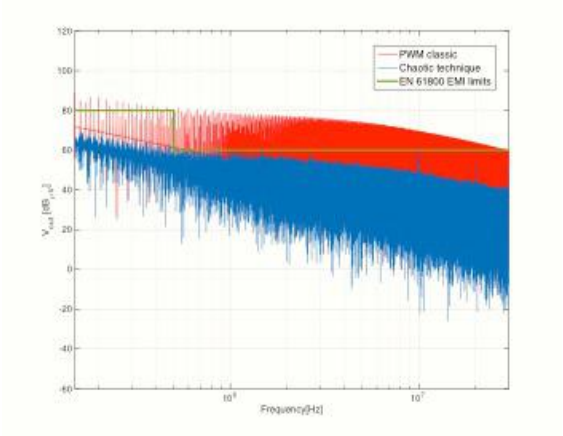

Fig.1 EMI of DC-DC Converter with Classic and Chaotic PWM, Compared with EN 61800 EMI Limits

Conclusion

In this paper a chaotic PWM switching technique for a DC-DC high boost converter with very low input ripple isTable 2. Parasitic parameters presented. The chaotic PWM allows obtaining an output EMI mitigation by spreading the output voltage power spectrum. In particular, the Chua's oscillator is used to generate an analog chaotic carrier waveform in Matlab-Simulik environment. A reduction of the harmonic content of the DC-DC converter output voltage has been verified respect to a traditional PWM control. Then, a HF model of the converter under study has been evaluated and the EMI mitigation has been demonstrated. More in detail, the simulation results show that the use of a chaotic PWM allows obtaining an EMI reduction of about 20 dBV.

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