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A 28GHz Power Amplifier with Analog Predistortion Linearizer in 65nm CMOS

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Abstract: This paper proposes that a radio frequency power amplifier is suitable for a 5G millimeter wave. It adopts a three-stage single-ended structure at 28GHz. An analog predistortion linearization method is used to improve the linearity of the power amplifier (PA). As a result, there is a significant improvement in power-added efficiency (PAE) and linearity is achieved. The Ka-band PA is implemented in TSMC 65nm CMOS process. At 1.2V supply voltage, the PA proposed in this paper achieves a saturated output power of 15.9dBm and a PAE of 16%. After linearization, the output power at the 1dB compression point is increased by 2dBm, with efficient gain compensation performance.

Keywords: Millimeter wave; Power amplifier; Predistortion linearization; CMOS

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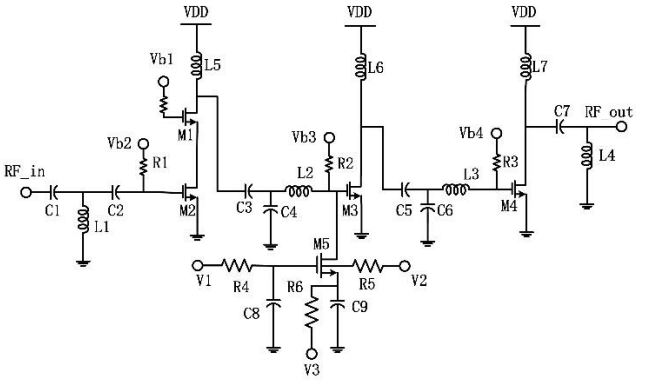
1 Introduction

In association with the rapid development of wireless communication technology, many complex modulation methods have been applied, thereby the transmission signal has a high peak-to-average power ratio (PAPR), and the PAPR signal is more likely to enter the saturation region and cause a nonlinear distortion. In order to improve the linearity, power back-off method can be used, but this reduces the working efficiency of the PA. “Doherty PA” is a method commonly used in recent years to improve efficiency when there is a power back-off [1].

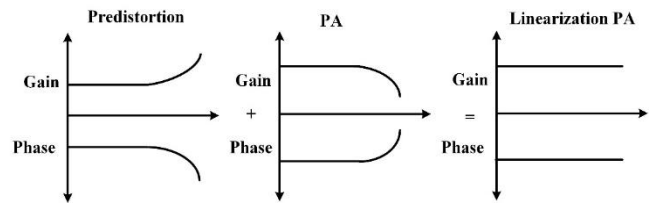
In addition with the application of 5G mobile communication technology, high bandwidth and high linearity of PA are required, thus power back-off cannot meet the requirements of high linearity. Therefore, there are many linearization techniques reported in recent state-of-the-art PAs. In exhibiting second-order intermodulation feedforward cancelling circuit, auxiliary path produces third-order intermodulation (IM3) distortion, by connecting in parallel with the main amplifier, the third-order components of the two cancels each other out[2]. However, the added auxiliary PA reduces the efficiency of the entire circuit and increase circuit cost. Predistortion linearizer is relatively simple to implement, and has a relatively wide dynamic range as well as operating bandwidth, which has gradually become the mainstream of linearization technology in millimeter wave frequency band. In a parasitic diode in the p-n junction of NMOS is used to form a linearizer, and added to the circuit, which can significantly cancel the IM3 terms[3]. In cold-mode MOS transistor has been used for MMW PA. It is a built-in linearization technology, which uses its nonlinear distortion characteristics to achieve addition compensation[4]. In order to meet the requirements of high linearity and improve the output 1dB compression point of output power, analog predistortion is a good choice. Cold-mode MOS transistor linearization method is easy to implement and can reduce chip area.

In this paper, a PA with enhanced cold-FET predistortion linearizer is implemented in 65nm CMOS process. A cold-mode MOSFET body bias circuit is placed in front of the driver stage transistor to compensate for the distortion characteristics of the PA. This linearization

technique improves the additional expansion capability of the circuit, and the linearity is also improved.



(a)



(b)

Figure 1. (a) Schematic of proposed PA with predistortion linearizer, (b) Predistortion structure schematic

2 Circuit Design

The schematic diagram of the proposed circuit is shown in Figure 1(a). This circuit adopts a three-stage single-ended structure, including a Cascode stage, and a two-level common source stage, composed of transistors M1, M2, M3, and M4. Common source structure can use lower supply voltage to achieve a higher voltage swing, the output stage adopts a common source structure to improve the output swing of the circuit, and the intermediate driver stage adopts a common source structure to drive the power stage. At high frequencies, due to the Miller effect caused by parasitic capacitance, the common source structure does not have high advanced characteristics. Therefore, the Cascode structure is added in the first stage to reduce the Miller effect, thereby increasing the benefits of the circuit, also improving the reverse isolation and stability of the overall circuit. Due to the high linearity of the Class A power amplifier, the three-stage amplifying structure all work in Class A, as well as the gate bias voltages Vb1: 0.75V, Vb2: 0.75V, Vb3: 0.8V and Vb4: 0.85V, respectively.

The matching network is achieved by inductance and capacitance. The output stage adopts an L-shaped matching network, which is simple in structure and easy to achieve, and has low loss to the output stage. The optimal load resistance of the power stage transistor is easily matched to the output load. The input stage adopts a T-shaped matching network. Conjugate matching is a very good application between stages, which can get better gain and efficiency. The series inductors (L2 and L3) are used in the inter-stage matching circuit to improve the circuit benefits.

Capacitors C1, C3, C5, and C7 are not only used as part of the matching network, but also used as DC block. C1 and C7 can prevent input and output signals from interfering with the circuit. C3 and C5 isolate the driver stage and the power stage, which can prevent the mutual influence between the stages, at the same time have the function of transmitting signals. In addition, they are responsible for the function of transmitting signals. The inductors L5, L6, and L7 are used as radio frequency (RF) choke to isolate the DC path and the RF path. It can inhibit high-frequency signals from entering the system. The value is slightly larger than that of ordinary inductors.

In order to meet the high linearity requirements of wireless communication systems, an analog predistortion linearizer circuit is used to improve the linearity of the PA. The basic principle is shown in Figure 1(b). A predistortion linearizer circuit is placed in front of the power amplifier, where it will produce a non-linear distortion, and the distortion characteristics are opposite to the PA. By using this structure, the gain and phase of the PA will be compensated, therefore the nonlinear distortion of the PA can be cancelled. The MOS transistor will produce nonlinear distortion during the cold mode operation. Therefore, the MOS transistor under this working condition can be regarded as an analog predistortion device to form an analog predistortion circuit. As shown in Figure 1(a), this analog

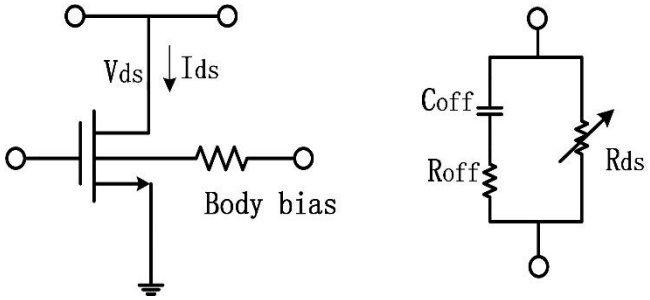
predistortion circuit is connected to the gate and source of the MOS tube by two bias resistors, as well as bypass capacitors are added to the gate and drain. Due to the parasitic capacitance of the cold-mode MOSFET, when the operating frequency increases, the added expansion capability will decrease, thus this kind of cold-mode MOS transistor predistortion circuit is often used in low-frequency circuits[5]. In order to improve the added expansion capability of the predistortion linearization circuit of the millimeter wave band PA, an enhanced cold-mode PA linearization circuit using body bias technology was proposed[6]. As shown in Figure 2, on the basis of cold-mode MOS predistortion, body bias technology is added to improve the added expansion capability of the circuit. The cold-mode predistortion linearizer can be equivalent to the capacitor C_{off} and the resistor R_{off} in series and then connected in parallel with the current source. The current source can be regarded as a variable resistor. Its DC-IV curve is shown in Figure 3. When the input power increases, the greater the dynamic range of R_{ds} changes, the stronger the added expansion capability is displayed. R_{ds} changes with the changes of V_{ds} and Ids, and the relationship between them can be expressed as,

$$|R_{ds}| = |\partial V_{ds}/\partial I_{ds}| \quad (1)$$

Where V_{ds} and I_{ds} are the drain-source voltage and current of the MOS transistor, respectively. It can be seen that R_{ds} is inversely proportional to the slope of the DC-IV curve. The smaller the R_{ds}, the larger the slope of the curve. The larger the linear range of the curve, the wider the range from linear to saturation, and the more obvious the predistortion characteristics. The stronger the added expansion capability.

As the R_{ds} decreases, the slope of the curve gradually increases, and the linear region of the curve becomes larger. The range from the linear region to the saturation region will be wider, the distortion characteristic will be more obvious, and the added expansion capability will be stronger. After adding the body bias resistor, it will increase the slope of the curve and increase the range of non-linear changes, thus having stronger distortion characteristics.

Figure 2. Equivalent circuit of proposed predistortion circuit



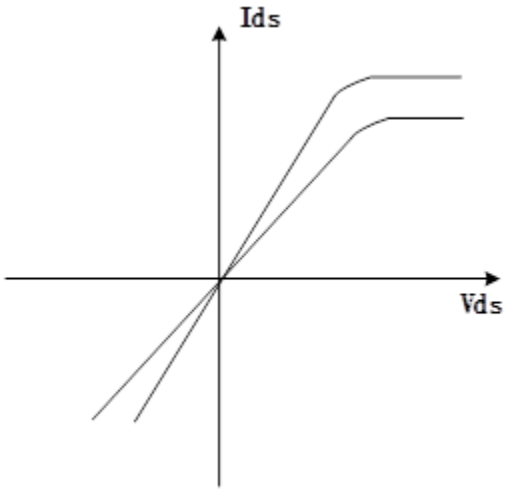


Figure 3. DC-IV curve

3 Simulation Result

The PA designed in this paper uses 1.2V power supply voltage and is realized by 65nm CMOS process. The simulated S-parameters of this PA with enhanced linearizer on and off are shown in Figure 4 and Figure 5. The input return loss S_{11} is affected slightly with linearizer on and off because of the input impedance of the linearizer, thus S_{11} reflection coefficient is small. However, the output return loss S_{22} has a certain offset. As shown in Figure 5, it can be seen that the small signal added has a large change. When the linearization is turned on, S_{21} is 25dB. When the linearization is turned off, S_{21} is reduced by 2dB due to the added expansion characteristics at 28GHz. The reverse isolation has not changed much and the overall isolation is better, as its less than -50dB.

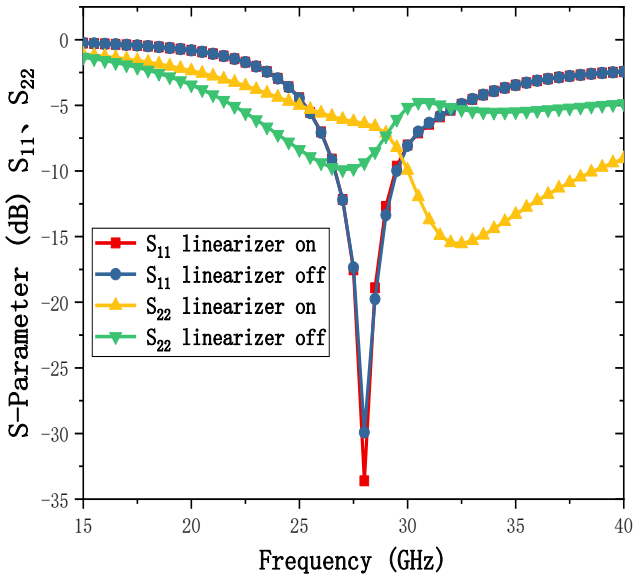


Figure 4. Simulated S_{11}, S_{22} of PA with linearizer on and linearizer off

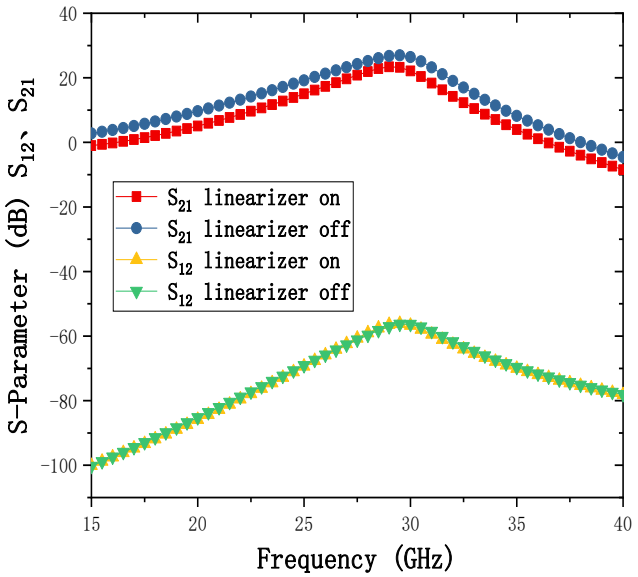


Figure 5. Simulated S_{12}, S_{21} of PA with linearizer on and linearizer off

Figure 6 shows the simulated large signal performance of this PA at 28GHz. When the enhanced linearizer is turned off, the saturation power is 15.3 dBm, with output power at the 1dB compression point (OP_{1dB}) of 11.9dBm. With the opening of linearization technology, the saturated output power is increased to 16dBm, and the output power at the 1dB compression point is 14 dBm. The result shows that the linearity has been improved, and P_{1dB} of PA has increased by 2dBm with linearizer on.

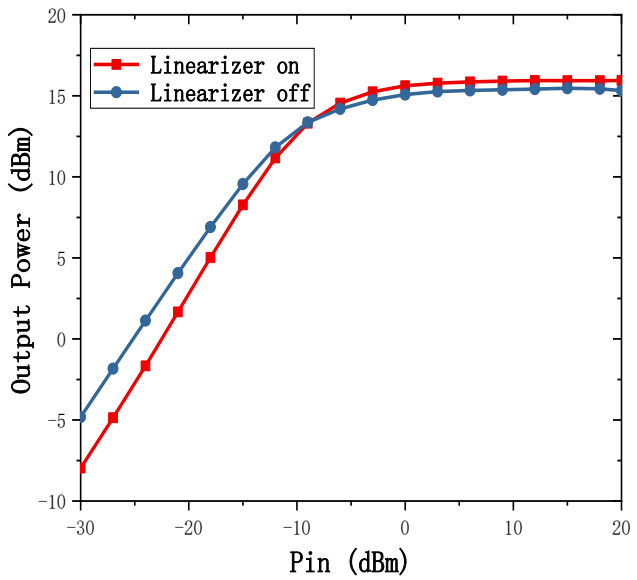


Figure 6. Simulated Pout of PA with linearizer on and linearizer off

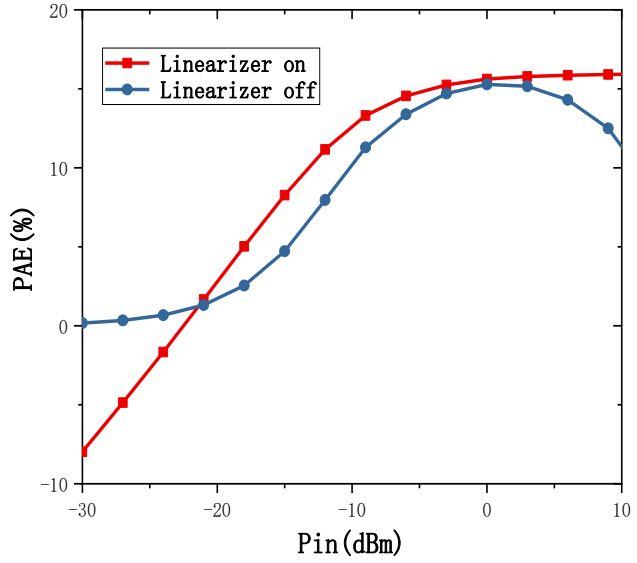


Figure 7. Simulated PAE of PA with linearizer on and linearizer off

Figure 7 shows the curve of efficiency versus input power. Before linearization is turned on, PAE has 15% peak PAE, and the efficiency at the input 1dB compression point is 9.2%. After linearization is turned on, PAE has a peak PAE of 16%, and the efficiency at the input 1dB compression point is 12.6%. Therefore, through analog predistortion linearization technology, the efficiency at the input 1dB compression point has been greatly improved. Table 1. shows a summary of the performance of the proposed PA and a comparison with a recently reported mixer operating in the Ka-band. We can

see that the proposed analog predistortion linearization method can improve the linearity of the PA while maintaining better gain characteristics.

Table 1. Performance Summary and Comparison with State-Of-The-Art PA

Ref	Process	Vdd (V)	Freq (GHZ)	Gain (dB)	P1dB (dBm)	Psat (dBm)	PAE_{max} (%)
1	65nm CMOS	2.5	28	21.1	19.84	21.4	15
2	90nm CMOS	-	60	13.1	18.9	18.9	-
3	180nmCMOS	1	23	12.8	15.8	18	15
4	28nm CMOS	1	30	15.7	13.2	14	35.5
5	65nm CMOS	1.1	28	15.8	14	15.6	41
This Work	65nm CMOS	1.2	28	25	14	16	16

4 Conclusion

This paper proposed a predistortion linearizer for millimeter wave CMOS PAs. The PA with the proposed linearizer implemented by 65nm CMOS process can provide PSAT of 15.9dBm and P1dB of 13.9dBm with a high gain of more than 20dB. It also has a peak PAE value of 16%. The proposed linearization technology has good added expansion capability which improves the output power and efficiency of the power amplifier to a certain extent

Disclosure statement

The author declares no conflict of interest.

References

[1]Nguyen H.T., Wang H. (2020), "A Coupler-Based Differential Millimeter Wave Doherty Power Amplifier with Impedance Inverting and Scaling Baluns," IEEE Journal of Solid-State Circuits, 55(5):1212-1223.

[2]Chen Y.H., Kao K., Chao C.Y., Lin K. (2015), "A 24 GHz CMOS Power Amplifier with Successive IM2 Feedforward IMD3 Cancellation," IEEE MTT-S International Microwave Symposium, Phoenix, pp. 1-4.

[3]Yeh J., Cheng J., Tsai J., Huang T. (2014), "A 57–66 GHz Power Amplifier with a Linearization Technique in 65nm CMOS Process," 2014 44th European Microwave Conference, Rome, pp. 1253-1256.

[4]Hsu Y., Kao K., Kao J., Tsai T., Lin K. (2013), "A 60 GHz CMOS Power Amplifier with Modified Predistortion Linearizer," 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, pp. 1-4.

[5]Tsai J.H., Chang H.Y., Wu P.S., Lee Y.L., Huang T.W., Wang H. (2006), "Design and Analysis of a 44-GHz MMIC Low-Loss Built-In Linearizer for High-Linearity Medium Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, 54(6):2487-2496.

[6]Tsai J., Wu C., Yang H., Huang T. (2011), "A 60 GHz CMOS Power Amplifier With Built-in Pre-Distortion Linearizer," IEEE Microwave and Wireless Components Letters, 21(12):676-678.

[7]Quadir N.A., Kashfi S., Jain A., Albasha L. (2019), "Millimeter-Wave Analog Predistorted Power Amplifier at 65nm Node," 2019 International Conference on Communications, Signal Processing, and their Applications (ICCSPA), Sharjah, United Arab Emirates, pp. 1-4.

[8]Weng S., Lee Y., Chen T., Liu J.Y. (2018), "A 60-GHz Adaptively Biased Power Amplifier with Predistortion Linearizer in 90nm CMOS," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, pp. 651-654.

[9]Huang T., Lin Y., Wang H. (2015), "A K-Band Adaptive-Bias Power Amplifier with Enhanced Linearizer Using 0.18μm CMOS Process," 2015

IEEE MTT-S International Microwave Symposium, Phoenix, pp. 1-3.

[10] Shakib S., Park H., Dunworth J., Aparin V., Entesari K. (2016), "A Highly Efficient and Linear Power Amplifier for 28GHz 5G Phased Array Radios in 28nm CMOS," IEEE Journal of Solid-State Circuits, 51(12):3020-3036.

[11] Ali S.N., Agarwal P., Gopal S., Heo D. (2019), "Transformer-Based Predistortion Linearizer for High Linearity and High Modulation Efficiency in Millimeter Wave 5G CMOS Power Amplifiers," IEEE Transactions on Microwave Theory and Techniques, 67(7):3074-3087.