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Design of a High-Voltage Constant-Voltage/Constant-Current Power Supply Based on a PSFB Topology and an Automatic Frequency-Conversion Strategy

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Abstract: To meet the requirements for wide-range output, current-limit protection, and stable closed-loop control in high-voltage capacitor charging, laboratory high-voltage sources, and pulse-power preamplifier systems, this paper presents a high-voltage constant-voltage/constant-current power supply based on a phase-shifted full-bridge (PSFB) topology. The supply operates from a typical 24 V low-voltage DC input and uses a 1:100 high-frequency transformer for isolated step-up conversion. Its output control range is 0–2200 V and 0–200 mA, with a rated power limit of 400 W. The controller uses an STM32G474CBT6, which generates four complementary phase-shifted gate-drive signals through the HRTIM module and samples secondary-side voltage, secondary-side current, primary-side current, auxiliary-supply status, and temperature feedback with an ADC synchronized to the switching cycle. The control algorithm calculates the constant-voltage, constant-current, and constant-power PI loops in parallel and selects the actual phase-shift duty cycle through minimum-duty-cycle arbitration. To reduce the efficiency fluctuation of fixed-frequency PSFB operation at very low and very high duty cycles, an automatic frequency-conversion strategy is introduced. Frequency increase or reduction within 11–45 kHz is selected according to the duty-cycle state, while score-counter hysteresis, a lockout window, and feedforward duty-cycle correction reduce the disturbance caused by frequency changes. Simulation and experimental results show that the prototype provides stable high-voltage output, constant-current charging, constant-voltage load operation, and ZVS turn-on, confirming its practical engineering value.

Keywords: PSFB; Phase-shifted full-bridge; High-voltage power supply; Constant-voltage/constant-current control; Automatic frequency conversion; ZVS

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1. Introduction

High-voltage isolated DC-DC power supplies are widely used in capacitor charging, insulation testing, laboratory high-voltage sources, and pulse-power devices. These applications require a wide output-voltage

range, clear current-limiting capability, and reliable protection during sudden load changes, output-capacitor charging, and abnormal operating conditions. Because of its strong isolation capability, moderate power rating, mature control method, and suitability for soft switching, the PSFB still has considerable value in medium- and high-power DC-DC converters. Research has shown that reconfigurable PSFB converters can extend the wide-voltage output range and are suitable for applications such as electric-vehicle charging [1]. However, conventional PSFB converters still suffer from an insufficient ZVS range, duty-cycle loss, circulating-current loss, and reduced synchronous-rectification efficiency under light-load and wide-load conditions. Researchers have addressed these issues through variable-inductor-assisted ZVS, light-load synchronous rectification, and improved ZVZCS structures [2–4].

In addition to topology, digital control strategies affect the efficiency and dynamic response of the PSFB. The switching frequency and phase-shift duty cycle jointly determine the energy-transfer window, switching losses, and operating state of the magnetic devices. Recent studies have used combined frequency-conversion and phase-shift control to optimize PSFB efficiency, while feedforward compensation has been applied to improve the dynamic response under peak-current-mode control [5,6]. Model predictive control and predictive deadbeat average control have also been used to improve the transient performance of PSFB and PSFB-CT converters [7,8]. Research on bidirectional PSFB control indicates that circulating current and reverse power must be actively suppressed through the modulation strategy [9]. These studies show that a high-voltage PSFB power supply cannot rely only on a fixed switching frequency and a single PI loop; instead, drive timing, synchronous sampling, mode switching, and frequency management must be considered together.

This study focuses on a high-voltage constant-voltage/constant-current power-supply application and designs a digitally controlled PSFB high-voltage supply based on the STM32G474CBT6. The main contributions are as follows: an isolated boost power stage is constructed with a 24 V input and an output of up to 2200 V; four complementary phase-shifted gate-drive signals are implemented through HRTIM; periodic synchronous sampling and multi-loop PI arbitration are used to achieve constant-voltage, constant-current, and power-limit control; an automatic frequency-conversion strategy is proposed to adjust the switching frequency according to the duty-cycle state; and the design is verified through simulation waveforms, efficiency distribution, strategy partitioning, ZVS waveforms, startup waveforms, and CV/CC load experiments.

2. Overall system design

The system provides an adjustable high-voltage DC output from a low-voltage DC input and supports configurable constant-voltage, constant-current, and power-limit operation over the full output range. The recommended input voltage is 24 V, with an allowable range of 18–28 V. The output voltage range is 0–2200 V, the maximum output current is 200 mA, the rated power limit is 400 W, and the switching frequency is controlled automatically between 11 and 45 kHz, with 35 kHz used as the reference frequency. The key design specifications are listed in **Table 1**. In addition to the rated specifications, maintainability during commissioning and application was considered. Voltage, current, and power settings can be configured through the communication interface, while protection thresholds and correction coefficients can be stored permanently to reproduce experimental conditions under different loads and test scenarios.

Table 1. Main electrical parameters of the system

Parameter	Numerical value or range	Description
Input voltage	18–28 V, 24 V typical	Low-voltage DC input
Output voltage	0–2200 V	Adjustable high-voltage DC output
Output current	0–200 mA	Constant-current limiting range
Output power	0–400 W	Constant-power limiting range
Switching frequency	11–45 kHz	Automatic frequency conversion range
Reference frequency	35 kHz	Default running frequency
Dead time	Approximately 200 ns	HRTIM complementary-output dead time
Main control chip	STM32G474CBT6	HRTIM and multiple ADC sampling
Transformer turns ratio	1:100	Isolation boost

The main power supply consists of a low-voltage input, a PSFB full bridge, a high-frequency transformer, a high-voltage rectifier and filter, and an output terminal (**Figure 1**). It isolates the low-voltage, high-current side from the high-voltage, low-current side, improving user and equipment safety while enabling independent feedback and discharge protection on the high-voltage side. The two bridge arms of the full bridge operate complementarily, and the effective energy-transfer time is adjusted through the phase shift between the leading and lagging bridge arms. The hardware control and protection structure is shown in **Figure 2**. The MCU performs drive generation, sampling, protection, and communication. The output voltage VSEC, secondary current ISEC, input voltage VPRI, primary DC IPRI_DC, primary AC IPRI_AC, auxiliary power supply, and temperature signals are collected. Hardware overcurrent protection uses a comparator and an HRTIM Fault input, allowing the drive to be shut down quickly outside the software control cycle.

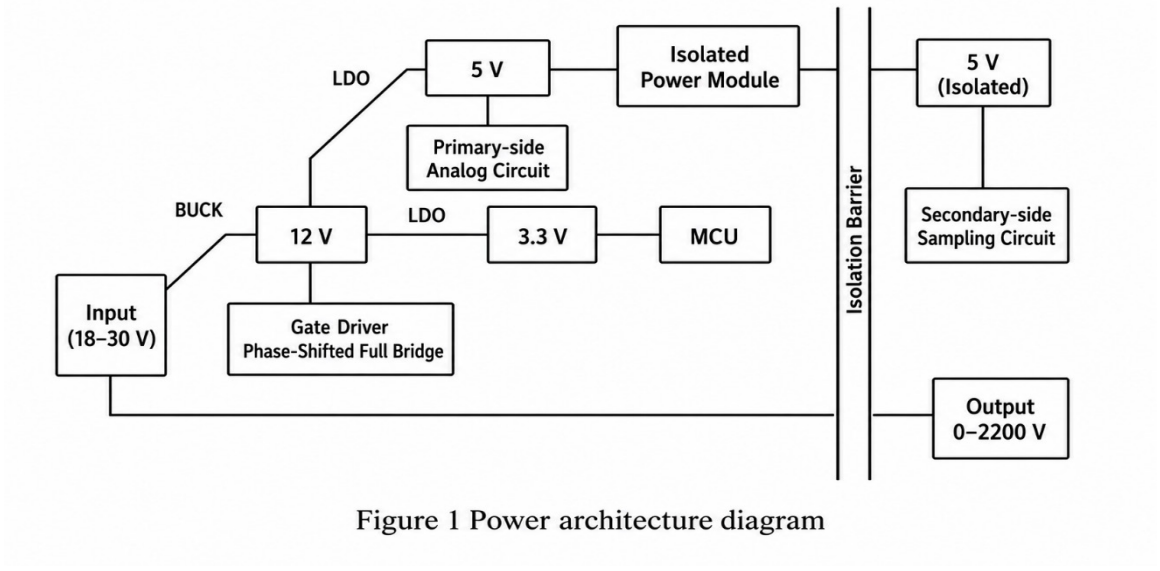

Figure 1 Power architecture diagram

Figure 1. Power architecture diagram.

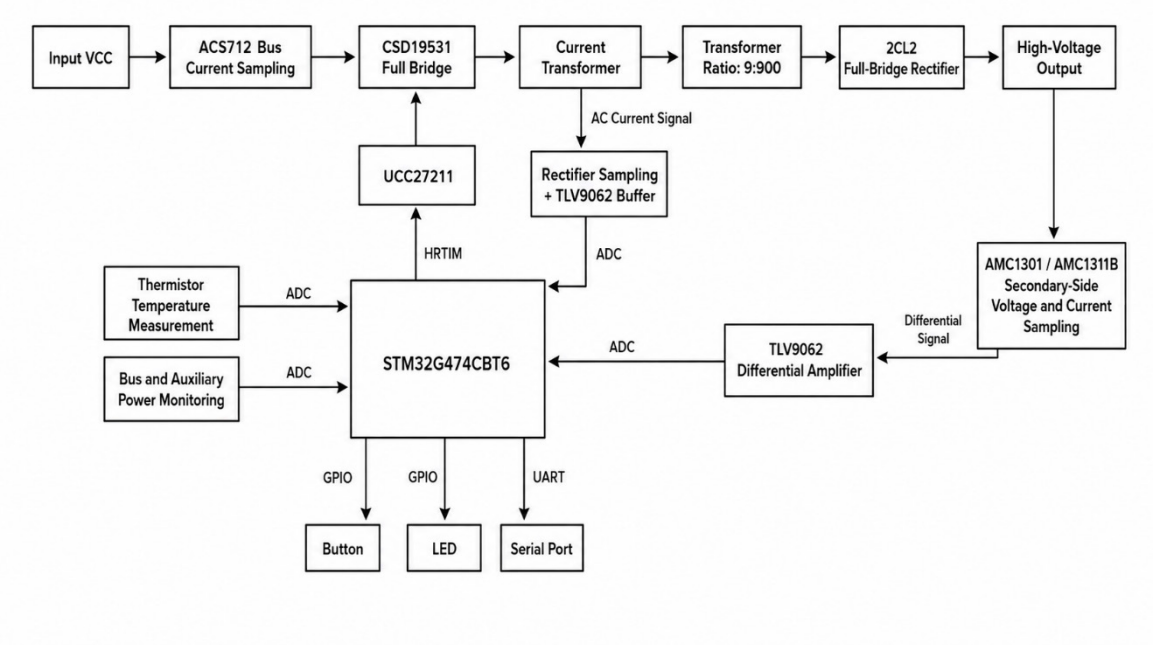

Figure 2. Hardware control and protection architecture diagram.

The phase-shift duty cycle is the key control variable of the PSFB. Let the switching period be and the effective phase-shift time between the two bridge arms be ; then, the normalized duty cycle is defined as:

$$d = \frac{2t_\phi}{T_s} = \frac{\phi}{\pi}, 0 \le d \le 1 \tag{1}$$

For the ideal output side, the output power is determined by the output voltage and output current:

$$P_o = V_o I_o \tag{2}$$

Because the PSFB provides high-voltage step-up conversion, the transformer turns ratio in this study is large; therefore, the secondary rectifier, capacitor, and sampling voltage-divider network must withstand high voltage. Insulation, output-energy storage, diode reverse stress, and feedback reliability require special attention.

In this study, the secondary-side output current is used for constant-current feedback; therefore, current-limit control is applied directly to the high-voltage-side load current rather than to an indirect estimate based on the primary input current.

3. Digital control method

Four complementary phase-shifted gate-drive signals are generated by the HRTIM module of the STM32G474CBT6. The HRTIM uses the master timer as the period reference, while Timer A and Timer B correspond to the two bridge arms. The compare registers define the trigger points for the bridge arms. When the frequency changes, the period register, sampling trigger point, and lagging-arm compare point are recalculated so that the gate drive remains synchronized with sampling. This approach supports variable-frequency operation between 11 and 45 kHz and makes fixed dead time and fault shutdown straightforward to implement in a high-voltage power supply.

Feedback sampling uses switching-cycle synchronization. Twenty-four sampling points are collected in each cycle, and the output voltage, secondary current, and primary current are averaged. Let there be M sampling points in the k th cycle, and let the j th sample of a feedback variable be $x_j(k)$; the cycle average is:

$$x_{avg}(k) = \frac{1}{M}\sum_{j=1}^{M} x_j(k), M = 24 \tag{3}$$

This method reduces the effects of switching-node oscillation, rectifier recovery, and high-voltage-divider noise. The output voltage VSEC is periodically averaged to suppress sampling disturbance; the output current ISEC serves as the main feedback signal of the constant-current loop; the primary-side DC IPRIDC is used for input-power estimation; and the primary-side AC IPRIAC is mainly used for peak monitoring and hardware overcurrent protection.

The control layer consists of three PI loops: constant voltage, constant current, and constant power. The loops compute their respective duty-cycle candidates in parallel, and the smallest candidate is selected as the actual control input.

$$d_{cmd}(k) = min\left\{d_{CV}(k), d_{CC}(k), d_{CP}(k), d_{max}\right\} \tag{4}$$

The underlying rule is “priority to the most restrictive constraint”. If the load current exceeds the set value, the constant-current loop reduces the duty cycle and takes over control; if the output approaches the target voltage, the constant-voltage loop takes over; and if the input or output power reaches its limit, the constant-power loop reduces the duty cycle. The system freezes the integrals of inactive loops to prevent drift. During soft start, the duty-cycle increase rate is limited, whereas the decrease rate is not, which balances smooth startup with a fast protection response.

4. Automatic frequency-conversion strategy

The fixed-frequency control structure is simple; however, it cannot cover the full high-efficiency operating range of an adjustable high-voltage output. Under low-output or light-load conditions, the duty cycle is low and little energy is transferred, while drive and magnetization losses remain. Under high-output or heavy-load conditions, the duty cycle approaches its upper limit and leaves insufficient control margin. The automatic frequency-conversion strategy uses the filtered duty cycle as the state variable. If the duty cycle is too low, the frequency is increased so that the operating point leaves the low-duty-cycle region; if the duty cycle is too high, the frequency is reduced so that the energy-transfer time per cycle increases. This logic is consistent with conclusions reported in a study on frequency-conversion-based PSFB efficiency optimization [5].

The automatic frequency-conversion parameters are listed in **Table 2**. The system reference frequency is set to 35 kHz, with an adjustment range of 11–45 kHz, and each adjustment step is limited to 1–4 kHz. Frequency reduction is triggered when the duty cycle exceeds 95%, with the target of reducing the predicted duty cycle to approximately 90%. The frequency-increase boundary depends on the current switching frequency so that low-duty-cycle operation does not persist for too long. To avoid frequent frequency jumps near the boundary, frequency-increase and frequency-reduction score counters and a lockout window are introduced. The system reloads the frequency only when the duty cycle remains in the corresponding region, and the score exceeds the threshold; it then enters a short lockout period during which no further frequency-conversion action is triggered.

Table 2. Automatic variable frequency control parameters

Parameter	Numerical value or rule	Function
Reference frequency	35 kHz	Default running frequency
Frequency range	11–45 kHz	Variable-frequency limit
Frequency step size	1–4 kHz	Single-step adjustment limit
Frequency-reduction trigger	d > 95%	Avoid high-duty-cycle saturation
Frequency-reduction target	Approximately d < 90%	Restore adjustment margin
Frequency-increase trigger	Low-duty-cycle region	Extend the light-load regulation range
Lockout window	100–200 ms	Suppress frequent switching
Feedforward exponent	$\gamma = 0.924$	Correct the duty cycle after frequency conversion

Changes in frequency affect the energy-transfer capability associated with a given duty cycle. If the frequency is changed while the duty cycle is kept unchanged, disturbances may appear in the output voltage and current. Therefore, this study uses feedforward duty-cycle correction to map the duty cycle at the old frequency to the initial duty cycle at the new frequency:

$$d_{ff} = \frac{2}{\pi} arcsin\left[clamp\left(sin\left(\frac{\pi d}{2}\right)\left(\frac{f_{new}}{f_{old}}\right)^{\gamma}, 0, 1\right)\right] \tag{5}$$

In this expression, f_{old} is the frequency before conversion, f_{new} is the target frequency, and is the feedforward exponent. After the frequency is reloaded, the integral term of the PI loop currently in control is synchronized near the feedforward duty cycle, reducing the transient disturbance caused by re-establishing the feedback loop. The benefit of feedforward compensation for the dynamic response of PSFB converters has also been verified in related studies [6].

5. Firmware and monitoring implementation

The system firmware consists of six modules: sampling, drive generation, control, configuration, protection, and communication. The sampling module triggers the ADC and aggregates data. The drive module provides HRTIM output, dead time, fault input, and periodic reload functions. The control module performs CV/CC/CP arbitration, soft start, and automatic frequency conversion. The configuration module stores PI parameters, frequency limits, soft-start step size, and calibration coefficients. The protection module manages hardware OCP, auxiliary-supply faults, overtemperature protection, and the watchdog timer; the communication module exchanges operating settings and telemetry data with the host computer through the serial port.

The host computer sets the target voltage, current limit, power limit, and running time, and reads the output voltage, output current, primary voltage, primary current, switching frequency, phase-shift duty cycle, operating mode, and protection flags. It does not participate in real-time closed-loop control; it is used only for parameter tuning and status monitoring. Real-time control is performed by the MCU, allowing the system to operate independently according to the stored parameters if communication is lost.

6. Simulation and experimental verification

To confirm that the power stage can operate across the automatic frequency-conversion range, a PSFB high-voltage step-up model was established for operating-characteristic analysis, including a low-voltage full bridge, step-up transformer, secondary high-voltage rectifier, and output filter network. In addition, experimental efficiency tests were carried out on the developed prototype, and 309 valid measured datasets were obtained. The tested frequencies covered approximately 10–50 kHz, while the designed operating range of this project was 11–45 kHz. The duty cycles covered 5–100%, the secondary voltages covered approximately 48.95–981.3 V, and the secondary currents covered approximately 10–198.8 mA. Since the primary-side current was acquired using an onboard Hall sensor, zero-offset and bandwidth-related errors may exist; therefore, the measured efficiency results were used mainly to analyze variation trends rather than as metrology-grade efficiency data. **Figure 3** shows that efficiency is strongly correlated with frequency and duty cycle. Lower efficiency appears in the low-duty-cycle region, while a large cluster of high-efficiency points appears in the medium- to high-duty-cycle region. **Figure 4** shows the partitioning of the automatic frequency-conversion strategy. The boundaries among the frequency-increase zone, stable zone, frequency-decrease maintenance zone, and frequency-decrease zone are clearly defined, preventing the system from remaining for long periods in unfavorable low- or high-duty-cycle regions.

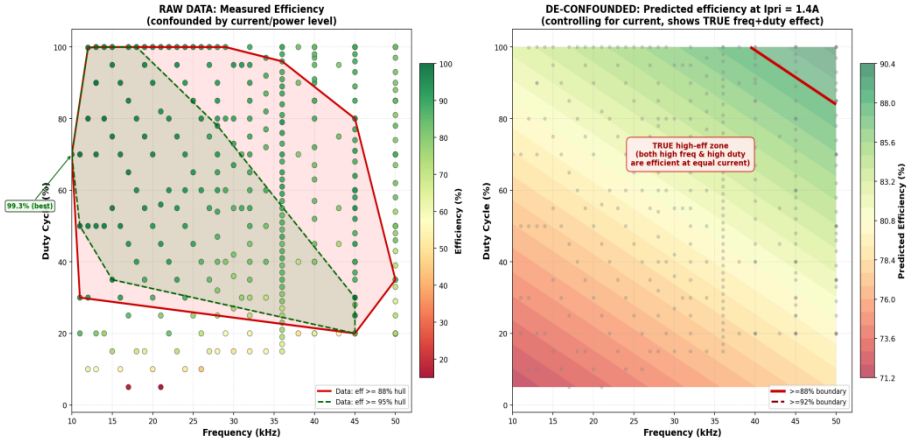

Figure 3. Frequency-duty cycle efficiency heat map and operating zones.

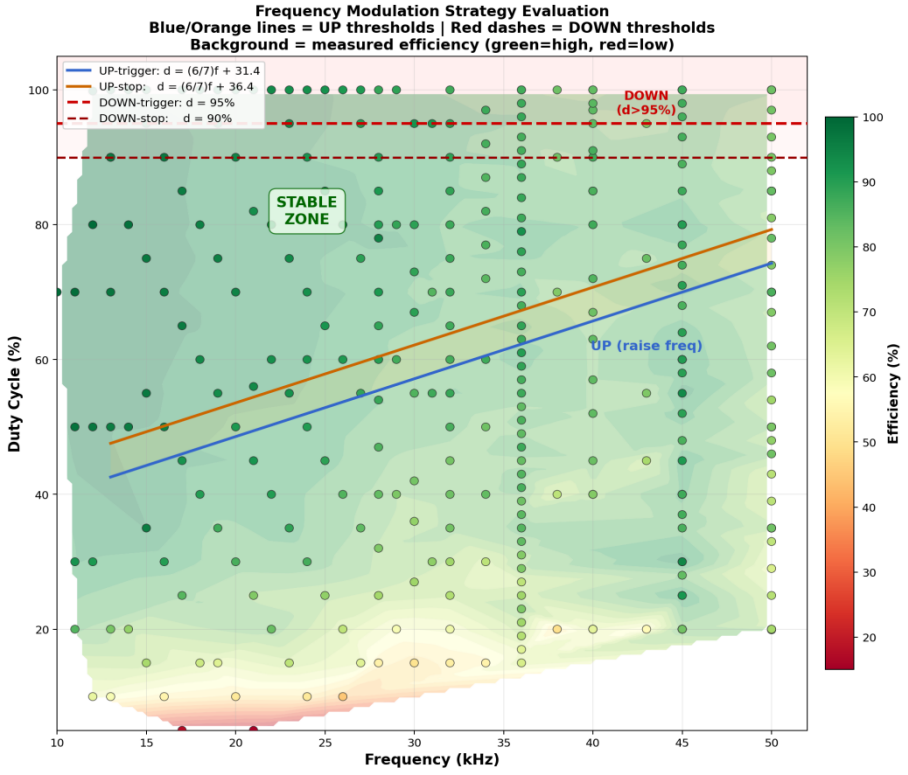

Figure 4. Automatic frequency conversion strategy zoning diagram.

ZVS is important for reducing switching loss in the PSFB. A previous study on full-bridge converters with a wide ZVS range indicates that the soft-switching range and filter requirements in variable-output applications affect efficiency and power density [10]. **Figure 5** shows the measured switching waveform of the prototype. Before the gate-drive signal arrives, the switching-node voltage falls close to zero, indicating that the MOSFET achieves near-zero-voltage turn-on under the tested conditions. This result shows that the designed power stage supports soft-switching operation and can operate over a wide frequency range under the automatic frequency-conversion strategy.

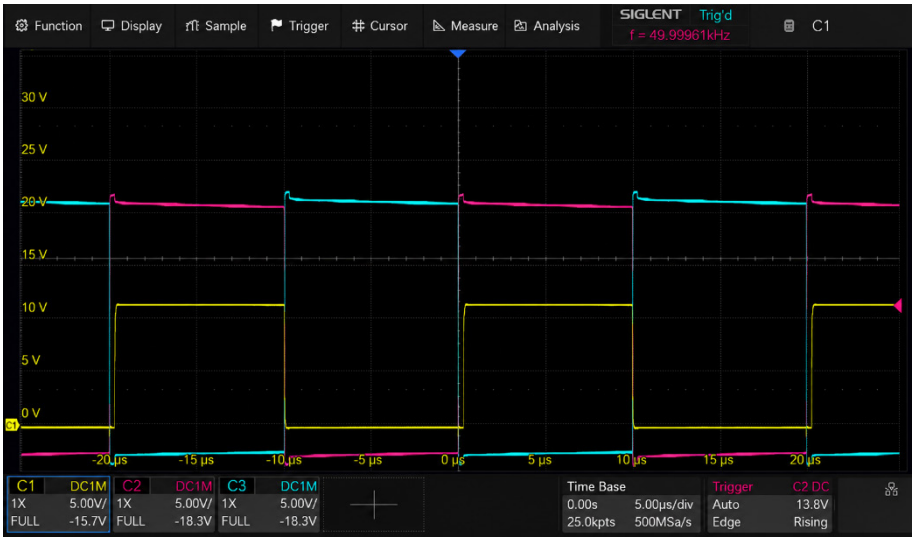

Figure 5. Measured waveform of ZVS on PSFB bridge arm.

The startup test confirmed the coordination between soft start and closed-loop control. **Figure 6** and **7** present the startup waveforms for 150 V and 230 V outputs, respectively; the output voltage rises along a controlled slope and settles near the target value. **Figure 8** and **9** show the ripple waveforms at these voltages, indicating that the system can maintain continuous voltage regulation under representative loads. Because of high-voltage safety requirements and probe limitations, full-scale ripple at kilovolt levels should be verified using a high-voltage differential probe.

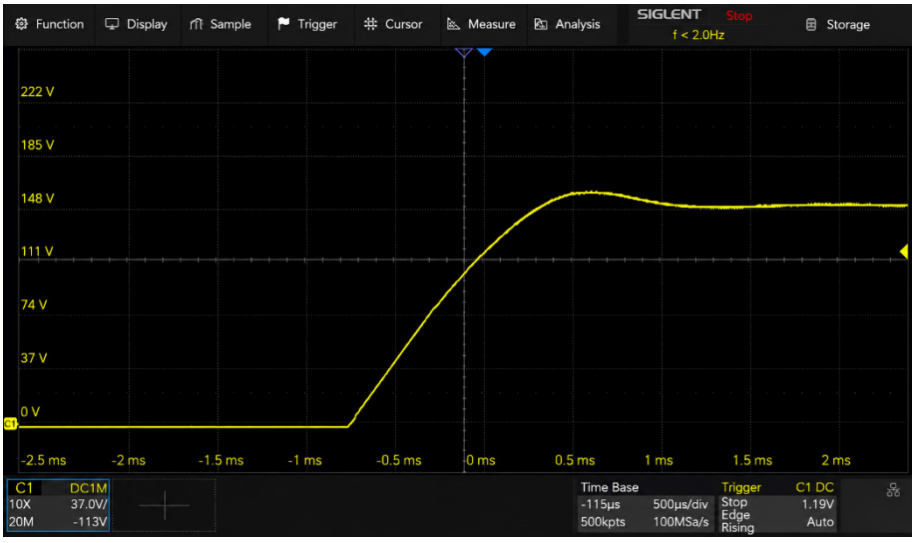

Figure 6. Startup waveform under 150 V output setting.

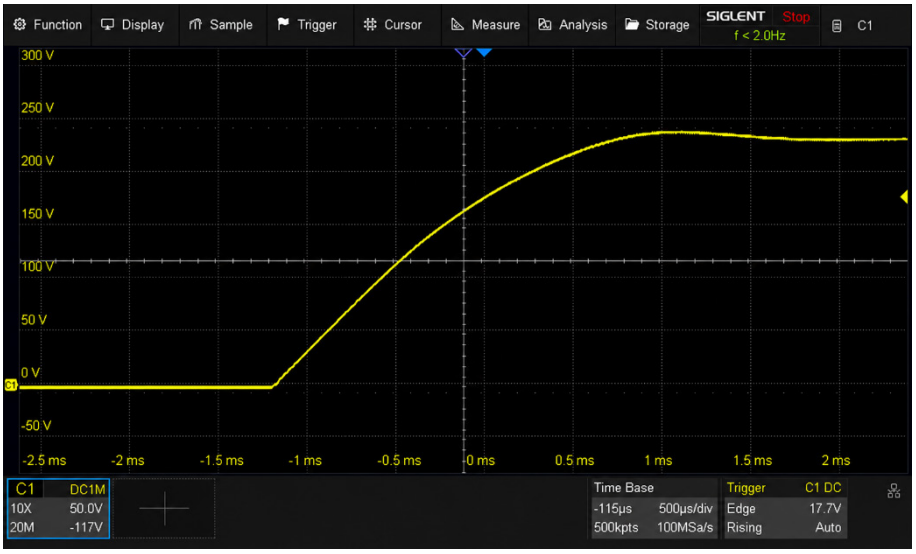

Figure 7. Startup waveform under 230 V output setting.

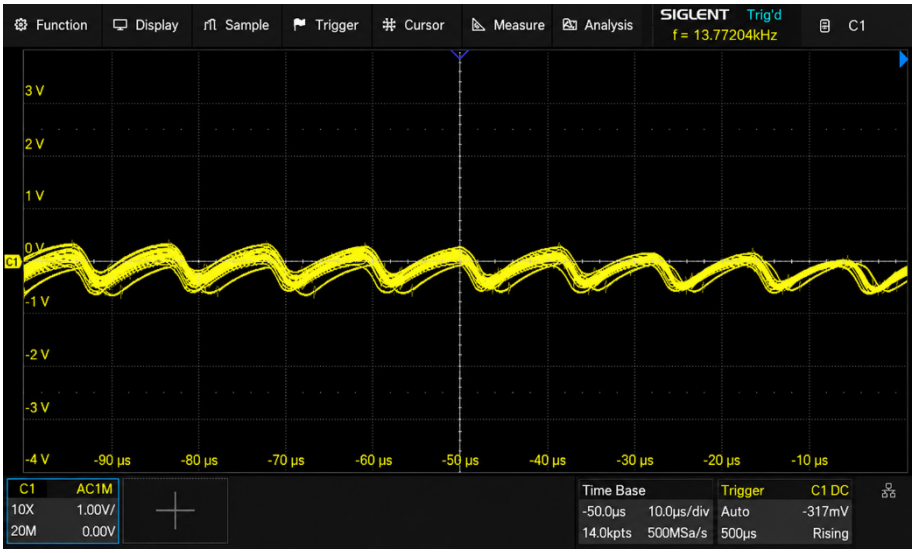

Figure 8. Voltage ripple waveform under 150 V output setting.

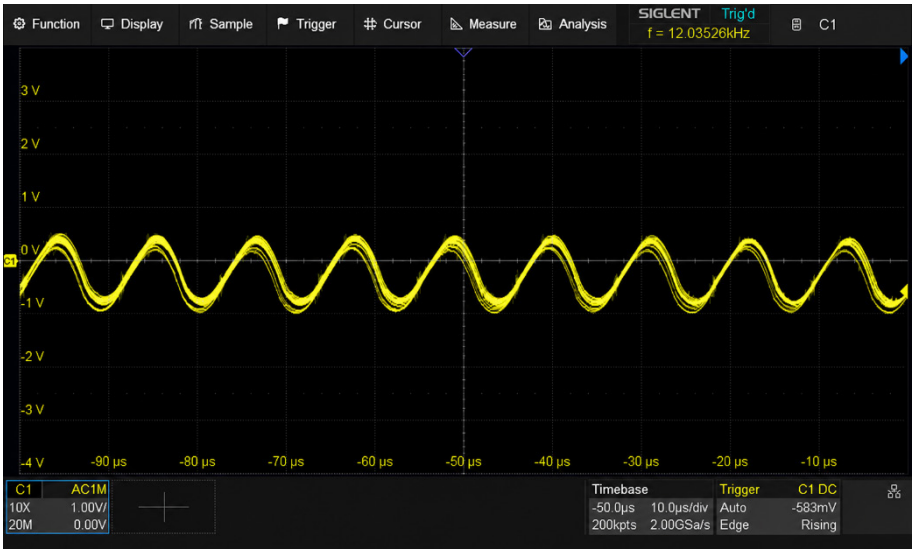

Figure 9. Voltage ripple waveform under 230 V output setting.

To verify the constant-current capability, two 1100 µF capacitors were connected to obtain an equivalent capacitance of approximately 550 µF. The target voltage was set to 2000 V, and the current limit was set to 200 mA. The test results are shown in **Figure 10**. The charging process took approximately 5.6 s, and the maximum output power was approximately 390 W, indicating that the CC loop can take over during the charging phase of the energy-storage load and transition smoothly as the output approaches the target voltage. To verify the constant-voltage capability, a 5 kΩ resistive load was used and the output voltage was set to 800 V. The test results are presented in **Figure 11**. The system can continuously provide a stable high-voltage output under load.

Figure 10. High-voltage capacitor constant current charging test.

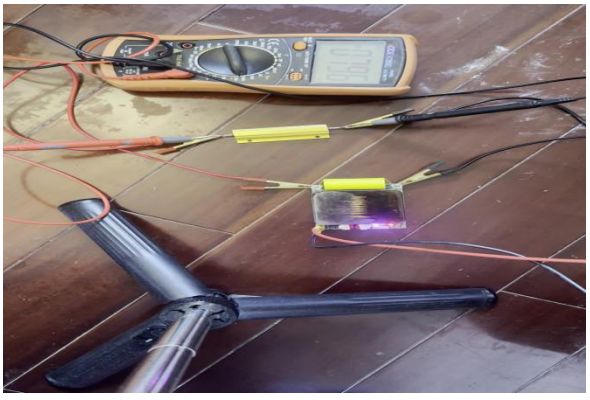

Figure 11. Constant voltage output test under resistive load.

7. Conclusion

This study designed a high-voltage constant-voltage/constant-current power supply based on a PSFB topology and an automatic frequency-conversion strategy. A typical 24 V low-voltage input and a 1:100 high-frequency transformer are used to achieve a maximum high-voltage output of 2200 V at 200 mA, with a 400 W power limit. Using the STM32G474CBT6 HRTIM module, the system generates four complementary phase-shifted gate-drive signals and performs periodic synchronous ADC sampling for voltage, current, auxiliary-supply, and temperature feedback. The parallel three-loop PI controller (CV, CC, and CP), minimum-duty-cycle arbitration, soft-start limiting, and integral freezing improve startup and mode-switching stability. To address the large variation in efficiency and regulation margin of fixed-frequency PSFB operation across a wide output range, an automatic frequency-conversion strategy based on duty-cycle status is proposed, with frequency ramp-up or ramp-down over 11–45 kHz. Disturbance during frequency conversion is reduced through score-counter hysteresis, lockout-window control, and feedforward duty-cycle correction. Simulations and experiments demonstrate stable high-voltage constant-voltage output, constant-current capacitor charging, ZVS turn-on, and low-ripple operation under representative working conditions. The system provides a digital control scheme with clear structure, configurable parameters, and good reproducibility for high-voltage capacitor charging and laboratory high-voltage power-supply applications.

Disclosure statement

The author declares no conflict of interest.

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