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A Study on the Influence of Stress State at the End of Dynamic Gate Biasing and Voltage Pre-Treatment on Threshold Voltage Shift in Silicon Carbide

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Abstract: This study focuses on the stress state of silicon carbide (SiC) power devices after the end of dynamic gate bias stress (DGS), and the influence mechanism of different pretreatments on the device threshold voltage (Vth) shift. Through a combination of experimental design and theoretical analysis, the impact of the instantaneous electric field distribution and charge trapping/release behavior at the end of dynamic gate bias on subsequent Vth stability was systematically explored. Research results show that the stress state (positive voltage/negative voltage) at the end of dynamic gate bias and whether pretreatment is performed will significantly affect the Vth shift of SiC devices under dynamic operating conditions. This research provides important theoretical basis and experimental guidance for the stability design and reliability improvement of SiC power devices.

Keywords: SiC device; Stress state; Threshold voltage

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1. Introduction

Silicon carbide (SiC), as a wide-bandgap third-generation semiconductor material, demonstrates immense application potential in high-frequency, high-temperature and high-power power electronics due to its excellent properties, including high breakdown field strength, high thermal conductivity and high electron saturation drift velocity. The threshold voltage (Vth) is a key parameter for devices such as silicon carbide power insulated-gate field-effect transistors (SiC power MOSFETs), and its stability is directly related to the device's switching characteristics, conduction losses and the control accuracy of the system [1]. In the 'Qualification of Power Modules in Automotive Power Electronic Conversion Units' (i.e. the automotive power module standard AQG324), the gate is aged using dynamic gate stress (DGS). This causes dynamic charging and discharging of interface traps and oxide layer traps, thereby inducing a significant shift in

Vth (ΔVth) to evaluate gate reliability. Although the mechanism of Vth shift under static gate bias stress has been extensively studied, the influence of the instantaneous stress state at the end of dynamic gate bias, specifically, the bias conditions at stress termination, on charge trapping/release kinetics remains unclear. Furthermore, the Vth shift following pre-treatment under different bias conditions at stress termination also requires further investigation [2]. Therefore, this study aims to: (1) elucidate the influence of the stress state at the end of dynamic gate bias on ΔVth in SiC devices, as well as the underlying mechanisms; (2) investigate the effect of pre-treatment on ΔVth in SiC devices. The findings of this study will provide a theoretical basis for reliability testing of high-performance SiC devices.

2. Experimental methods

2.1. Definition and extraction methods of threshold voltage

In this experiment, the threshold voltage was extracted using the constant-current method described in JEP183, as shown in **Figure 1**, where a constant current source is applied to the gate-drain (GD) short circuit, and the gate voltage corresponding to the gate-source (GS) voltage is measured as Vth.

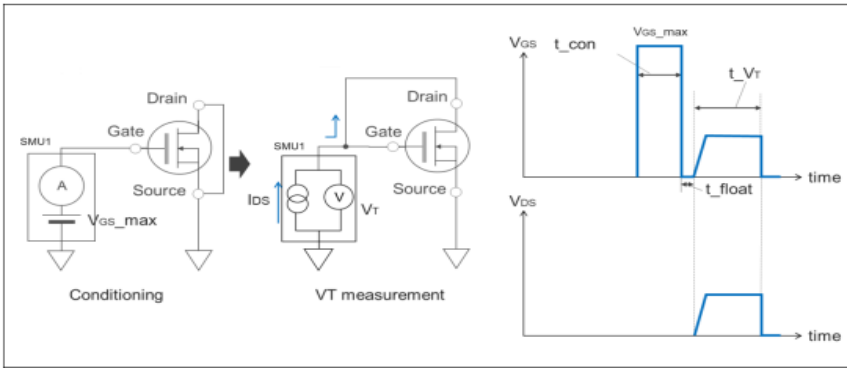

Figure 1. Schematic diagram of threshold voltage extraction using the constant current method [3].

2.2. Dynamic grid-shift stress (DGS) test protocol

Dynamic gate stress involves applying a periodic square-wave voltage signal to the gate, whilst the source and drain are short-circuited and grounded. A SiC MOSFET of model S1M040120H was used as the test specimen; its recommended gate voltage range is +15 V to -4 V, with a threshold voltage of approximately 2.8 V. The DGS test parameters are set as follows: the high level of the square wave signal is set to +15 V; the low level is set to -4 V, with a frequency of 170 kHz, 10^11 cycles, and dv/dt > 0.5 V/ns, satisfying the requirements of AQG324 for dynamic gate bias.

Variables for the end-of-stress state of dynamic gate bias: The dynamic gate bias stress sequence is terminated at either the high level (Vgh) or low level (Vgl) of the square wave, each maintained for 1 ms.

The experimental procedure is as follows:

(1) Measure the initial threshold voltage Vth_initial;

(2) Apply the dynamic gate bias stress with the set parameters to the device immediately upon the conclusion of the dynamic gate bias stress, fix the gate voltage at the preset high level or low level;

(3) Remove the gate voltage stress, allow the device to stand for 1 hour, measure the post-stress threshold voltage Vth_stressed, and calculate ΔVth.

This experiment was conducted using four samples, with the threshold voltage drift under different stress conditions recorded separately.

2.3. Voltage pre-conditioning protocol for threshold voltage

Voltage pre-conditioning is performed prior to threshold voltage testing. This experiment utilises positive gate voltage pre-conditioning: a positive DC voltage Vpre+ is applied to the gate, with the source and drain shorted to ground, for a pre-conditioning duration of 10 ms [4]. Vpre+ is set to the positive value of the dynamic gate bias, i.e. +15 V. Specifically, the difference between VTH measured after pre-conditioning following the end of the final positive pulse of the DGS and VTH measured directly after the end of the final negative pulse of the DGS is analysed to assess the impact of pre-conditioning on the threshold voltage recovery behaviour. Similarly, four samples were used for comparative testing.

3. Results

Taking the case where a positive bias is applied after DGS completion followed by a threshold voltage test as an example, the overall waveform is shown in **Figure 2**; schematic diagrams and final experimental results for the other experimental schemes are also presented.

Figure 2. Threshold voltage test following positive bias after DGS completion.

3.1. Impact of high-level dynamic gate bias (+15 V) on VTH without pre-treatment

The dynamic gate bias ended at a high level (+15 V), and no pre-treatment was performed prior to the threshold voltage (VTH) test. The test results are shown in **Figure 3** and **Table 1**.

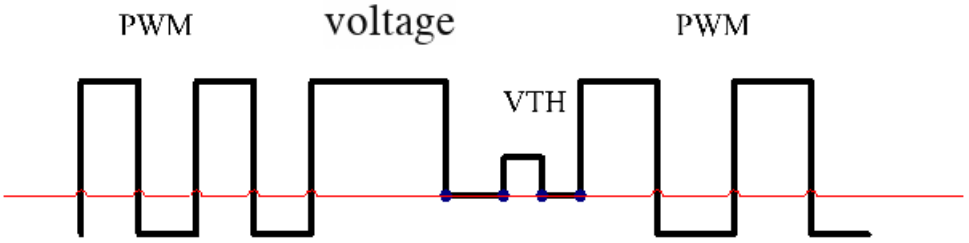

Figure 3. PWM signal around the threshold voltage (VTH).

Table 1. Test results when dynamic gate bias ends at a high level

No.	VGS (th) before test	VGS (th) after test	Rate of change
1	2.8237	2.90733	2.96%
2	2.848975	2.952255	3.63%
3	2.81844	2.931785	4.02%
4	2.941895	2.91958	-0.76%

3.2. Impact of low-level dynamic gate bias (-4 V) on VTH without pre-conditioning

The test results when the dynamic gate bias ends at a low level (-4 V) are as follows. The dynamic gate bias ends at a low level (-4 V), and no pre-conditioning was performed during the threshold voltage VTH test; the test results are shown in **Figure 4** and **Table 2**.

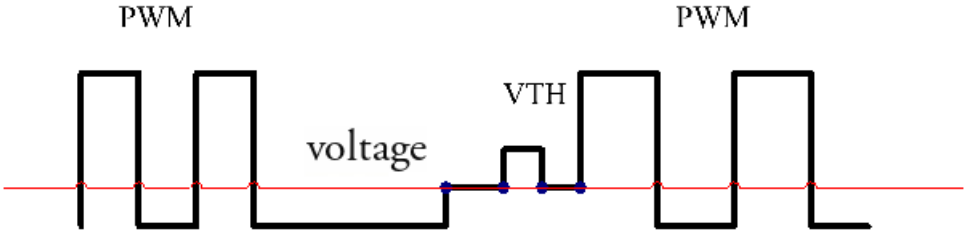

Figure 4. Transition between PWM and constant-voltage operation.

Table 2. Test results when dynamic gate bias ends at a low level

No.	VGS (th) before test	VGS (th) after testing	Rate of change
5	3.012025	3.0557	1.45%
6	2.92808	2.98728	2.02%
7	2.94193	2.955055	0.45%
8	2.90291	2.9165	0.47%

3.3. VTH stability under +15 V dynamic gate bias with pre-conditioning

The dynamic gate bias ends at a high level (+15 V) and was pre-conditioned prior to the threshold voltage (VTH) test; the test results are shown in **Figure 5** and **Table 3**.

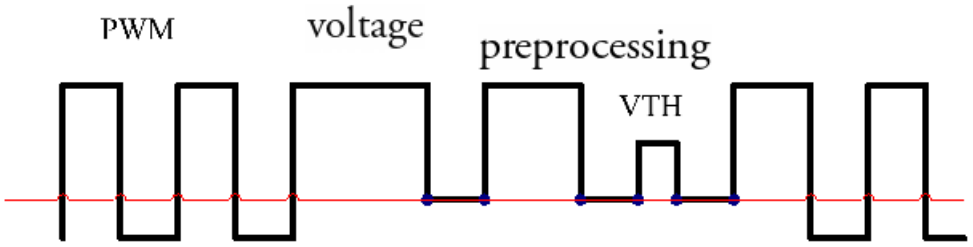

Figure 5. PWM-Voltage-Preprocessing-PWM control scheme.

Table 3. Test results following pre-processing after dynamic gate bias termination at a high level

No.	VGS (th) before test	VGS (th) after test	Rate of change
9	2.8853	2.94079	1.92%
10	2.93096	3.0054	2.54%
11	2.91668	2.97624	2.04%
12	2.953975	3.022735	2.33%

3.4. VTH stability under -4V dynamic gate bias with pre-processing

The dynamic gate bias ends at a low level (-4 V), and pre-processing was performed during the threshold voltage (VTH) test. The test results are shown in **Figure 6** and **Table 4**.

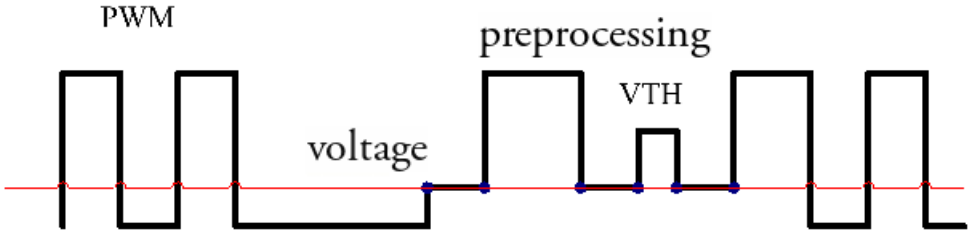

Figure 6. Pulse-width modulation (PWM) signal preprocessing and thresholding waveform.

Table 4. Test results following pre-processing after dynamic gate bias termination at a low level

No.	VGS (th) before test	VGS (th) after test	Rate of change
13	2.917325	2.97936	2.13%
14	2.91215	2.991115	2.71%
15	2.905615	2.954775	1.69%
16	2.90733	2.971925	2.22%

4. Discussion

4.1. Effect of dynamic gate bias end stress state on threshold voltage offset

Tables 1 and **2** show the threshold voltage offset ΔVth corresponding to different final gate voltage

amplitudes Vg_end. It can be seen from the figures that when the dynamic gate bias stress ends at a high level (Vg_end = 15 V), the device exhibits a positive threshold voltage offset (ΔVth > 0), with a relatively large absolute value. When the dynamic gate bias stress ends at a low level (Vg_end = −4 V), the device exhibits a positive threshold voltage offset (ΔVth > 0), with a smaller absolute value. However, the offset values for both cases are unstable; **Table 1** shows a difference of 4.78% between the maximum and minimum offsets; **Table 2** shows a difference of 1.55% between the maximum and minimum offsets. The threshold voltage offsets are shown in **Figure 7**. It can be seen that the threshold voltage offsets after pre-treatment are more stable than those without pre-treatment, and the offsets ending at a high level are significantly larger.

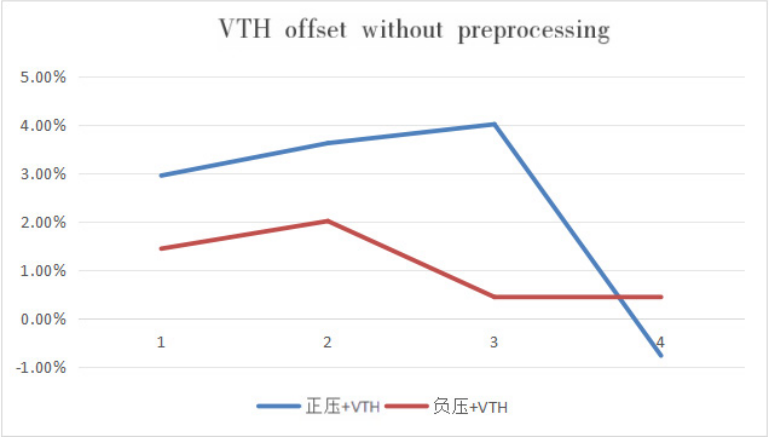

Figure 7. Comparison of threshold voltage offsets after dynamic gate bias without pre-processing.

This phenomenon can be explained by the gate oxide/interface charge trapping model. When the dynamic gate bias stress ends at a higher forward gate voltage Vg_end, electrons in the gate oxide acquire higher energy and are more likely to tunnel into trap levels or interface states within the gate oxide, forming fixed positive charges or negative interface trap charges. As fixed charges are captured by traps, the curve shifts as a whole, resulting in a larger Vth offset. Concurrently, a lower Vg_end may promote the injection and trapping of holes, or cause the partial release of trapped negative charges, thereby activating interface states or near-interface traps, which in turn reduces the magnitude of ΔVth. Consequently, the voltage level at the conclusion of the dynamic gate bias directly influences carrier injection capability and trap-trapping behaviour [5–7].

4.2. Effect of voltage pre-treatment on threshold voltage offset

Tables 3 and **4** show the measured effects of the forward gate voltage pre-treatment Vpre+ on the threshold voltage Vth offset. Compared with the untreated control group (**Tables 1** and **2**), appropriate forward gate voltage pre-treatment effectively suppresses the instability of ΔVth, with the threshold voltage offset shown in **Figure 8**. It can be clearly seen that, following pre-treatment, the Vth drift in both experimental groups is relatively stable and shows no significant difference. This indicates that forward gate voltage pre-treatment can reduce the amount of charge that can be trapped under subsequent dynamic gate bias stress by pre-filling some deep traps or passivating some active interface states, thereby improving the stability of the threshold voltage drift.

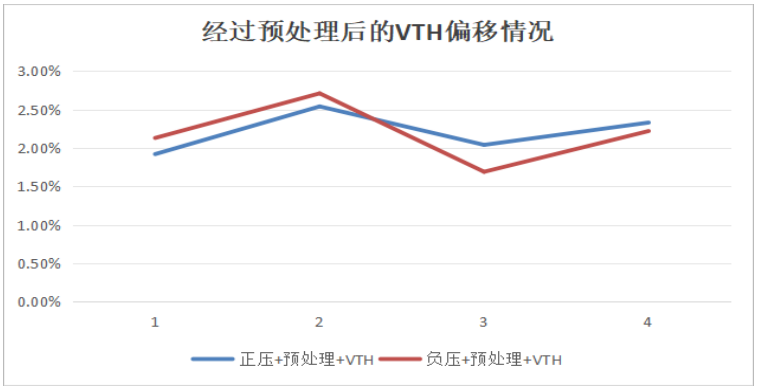

Figure 8. Comparison of threshold voltage offsets following dynamic gate bias and pre-processing.

5. Conclusion

The instability in the threshold voltage (Vth) induced by negative bias stress primarily stems from the capture and emission processes of holes in shallow energy level traps. This process is a rapid and reversible mechanism, rather than a permanent degradation caused by interface states. The variation in threshold voltage (ΔVth) can be stabilised through pre-treatment methods. The parallel shift in the curve induced by positive gate voltage stress is likely due to the capture of electrons by deep-level traps. Given that these are deep-level traps, ΔVth can similarly be stabilised through pre-treatment methods. Transient effects arising from the final stress applied immediately prior to testing (particularly the easily reversible hole trapping phenomenon induced by negative stress) play a dominant role in the measurement results. Consequently, applying a dual-gate stress (DGS) with a 'negative gate voltage tail' reduces the ΔVth shift. However, the positive Vth drift caused by positive stress is far greater than the negative Vth drift caused by negative stress. In other words, in DGS stress tests where positive and negative stresses are applied alternately, over time, the stable, cumulative electron capture effect induced by positive stress gradually becomes dominant, thereby masking the transient effects induced by negative stress. Consequently, in the long term, the total Vth drift is determined by the dominant positive drift mechanism; regardless of the final stress polarity, the value ultimately converges to the same stable value following pre-conditioning.

Disclosure statement

The author declares no conflict of interest.

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