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Research on ESD and TVS Protection Technology in Semiconductor IC Package Test

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Abstract: With the development of the semiconductor process to 5 nm and below, ESD protection faces challenges. The TVS reduces the response time to 0.5 ns through the three-dimensional TSV structure, and the SiC / GaN material achieves high temperature protection of 200℃ and 15 kV. The multi-stage cooperative protection network combined with inverted welding and flexible substrate technology meets the IEC 61000-4-2:2024 and AEC-Q100-012 standards. The parasitic inductance was suppressed to < 0.05 nH in high-frequency scenarios, and the eWLB package verified the technical feasibility. Two-dimensional materials and intelligent monitoring system promote the evolution of ESD protection to the system level.

Keywords: ESD protection; TVS structure; System-level protection

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1. Introduction

As semiconductor process nodes advance to 5 nm and below, the miniaturization and high-density integration of integrated circuits have posed unprecedented challenges to electrostatic discharge (ESD) protection. ESD events generate transient voltages reaching thousands of volts, with energy density increasing exponentially in miniaturized devices, easily causing gate dielectric breakdown, metal interconnect fusing, and other damage. Approximately 70% of ESD damage is latent, where device functionality remains temporarily normal but reliability degrades. Such damage is difficult to detect in conventional testing and may lead to catastrophic failures during the product lifecycle. Practice shows that relying solely on traditional external TVS devices in packaging is no longer sufficient for high-frequency and high-speed scenarios. Multi-level ESD protection networks must be integrated at the chip design stage, with parasitic parameter control optimized through packaging processes.

2. Basic principles of ESD and TVS protection technologies

2.1. Generation mechanism and hazards of ESD

ESD protection must comply with the ANSI/ESD S20.20-2023 standard, requiring surface resistivity control of 10^6–10^9 Ω/sq for 2.5D/3D packaging workstations to balance electrostatic dissipation and signal integrity. Charge discharge paths are quantified through HBM (Human Body Model), MM (Machine Model), and CDM (Charged Device Model). The HBM model reveals the destructiveness of high-voltage events (e.g., 8 kV) on metal interconnects: transient high currents trigger Joule heating effects, causing aluminum interconnect temperatures to rise abruptly above 800°C, ultimately leading to fusing or PN junction burnout [1]. Beyond thermal damage, strong electric fields can directly break down ultra-thin dielectric layers (e.g., 1 nm gate oxide), triggering tunneling effects at tens of volts and causing threshold voltage drift or permanent failure. Node scaling (e.g., FinFET and GAA architectures) exacerbates ESD vulnerability, as reduced metal linewidths and thinned dielectrics decrease withstand voltage by about 30%, while complex three-dimensional structures hinder precise control of charge paths. To address this, optimization should focus on materials (low-resistance, high-withstand-voltage substrates), design (chip-level ESD protection circuits), and processes (protective module integration compatible with FinFET/GAA) to enhance device antistatic capability while maintaining performance.

2.2. Working principle of TVS

TVS achieves ESD energy absorption through nonlinear volt-ampere characteristics, with core structures including PN junctions, multilayer varistors (MLV), and multi-level protection networks. Operation is based on avalanche breakdown: when reverse voltage exceeds the breakdown voltage (VBR), the TVS rapidly enters a low-resistance state, clamping the transient voltage within a predetermined clamping voltage (VC) range (VBR-to-VC ratio typically 1.2–1.5), protecting downstream circuits from overvoltage damage. Multi-level protection networks employ a “coarse-fine” architecture, where the first-level TVS (response time < 1 ns) absorbs most ESD energy with high conduction speed, and the second-level RC filtering network further suppresses residual voltage fluctuations. For high-frequency scenarios, three-dimensional stacked TVS shortens current paths to the micrometer level via vertical interconnects (e.g., through-silicon vias, TSV), reducing parasitic inductance below 0.1 nH and improving clamping efficiency by 40%, significantly decreasing signal reflection and impedance mismatch. Silicon carbide (SiC) TVS, with its 3.26 eV wide bandgap, can withstand 15 kV ESD impacts at 150°C, complying with AEC-Q101 automotive standards. Key parameters (e.g., dynamic resistance, junction capacitance) must be optimized based on application needs (e.g., operating frequency, temperature range) to balance ESD protection and signal integrity requirements [2].

3. ESD protection technologies in packaging and testing

3.1. Analysis of ESD risk points in packaging and testing processes

In packaging and testing, ESD risk points include: bare dies losing protection after wafer dicing, CDM discharge easily occurring during packaging, high electrostatic voltages potentially generated during ATE operations, high electrostatic sensitivity in high-speed interfaces and RF chips, and electrostatic accumulation due to poor grounding or prolonged ionization equipment decay times. CDM testers must be upgraded, following standards such as ANSI/ESD SP17.1, with coordinated prevention using ion fans, ESD workstations, and other equipment to ensure safe and reliable packaging and testing.

3.2. Key parameters and testing methods for ESD protection design

ESD protection must strictly comply with the IEC 61000-4-2:2024 standard, meeting stringent requirements of 8 kV contact discharge and 15 kV air discharge, while monitoring key parameters: clamping voltage level (VCL), peak current (IPP), and energy (W) [3]. Failure modes are divided into hard failures (e.g., leakage current > 1 μA causing permanent device damage) and soft failures (e.g., DDR5 interface timing deviation tAC ± 5% causing functional anomalies). For precise localization of current distribution within packages, 3D-TLP (Transmission Line Pulsing) technology identifies high-density current hotspots (e.g., up to 10^6 A/cm^2 at QFN package bond wires), reducing current density to < 5×10^5 A/cm^2 through optimized TVS layout (e.g., shortened paths or added parallel branches) to suppress local overheating and breakdown risks. The ANSI/ESDA STM5.5.1-2024 standard introduces mmWave-band ESD testing, using vector network analyzers (VNA) to quantify signal integrity failures with ΔS21 > 1 dB, driving protection design evolution toward high-frequency characteristics. Clamping speed (< 1 ns), low parasitic inductance (< 0.1 nH), and broadband impedance matching must be balanced to meet new ESD robustness challenges in 5G/6G communications and high-speed optical modules.

4. Design and packaging integration technologies for TVS devices

4.1. Optimization design methods for TVS devices

TVS achieves low junction capacitance (0.1 pF) through gradient-doped PN junctions and Schottky contact structures, meeting USB4 20 Gbps high-speed interface requirements, while multi-finger strip layouts optimize current distribution, improving uniformity by 60% and withstanding 100 A surges. Multi-level protection circuits employ a “coarse protection-fine filtering” architecture, with the first-level TVS responding within 0.5 ns to discharge 90% of ESD energy, and three-level protection elevating 28 nm chip HBM antistatic levels from 2 kV to 8 kV [4]. In materials, silicon-based TVS is cost-effective for low-voltage scenarios but limited in high-voltage applications; gallium nitride (GaN) devices, with low dynamic resistance (0.05 Ω), suit 5G mmWave high-frequency needs; SiC withstands 15 kV ESD impacts at 200°C, complying with AEC-Q101 automotive standards. Three-dimensional packaging optimizes stress distribution via TSV, reducing interfacial thermal resistance by 30% and meeting JEDEC temperature cycling test requirements, addressing thermal management and reliability challenges in high-integration packages.

4.2. Integration technologies of TVS in packaging

4.2.1. Comparison between on-chip integration and off-chip discrete schemes

On-chip TVS achieves near-end interconnection with core circuits via back-end-of-line (BEOL), following the “near-end protection” principle by placing devices within 5 μm of I/O pads, reducing signal transmission delay to 50 ps but at the cost of 12–15% increased chip area. In contrast, off-chip discrete TVS uses Flip-Chip packaging and μBump arrays, meeting 56 Gbps SerDes interface impedance matching needs through parasitic inductance control (< 0.2 nH). Experiments show superior performance in 32 Gb/s GDDR6 interfaces, signal return loss (S-parameter return loss < -15 dB) significantly better than on-chip schemes, validating the advantages of discrete structures for signal integrity in high-frequency scenarios, especially suitable for area-sensitive systems requiring both high bandwidth and low loss [5].

4.2.2. Thermal management and signal integrity assurance

TVS thermal accumulation issues are mitigated through packaging heat dissipation design: QFN-embedded copper

pillar arrays reduce thermal resistance from 80°C/W to 35°C/W; 2.5D packaging silicon interposer microchannels control hotspot temperatures below 85°C. High-speed signal links require TVS placement away from PLL clock lines, with differential symmetric routing limiting parasitic capacitance imbalance to ± 2 fF. The IEEE 1149.13-2024 standard requires 112 Gbps PAM4 interface TVS schemes to pass TDR verification with $\Delta Z < \pm 5\ \Omega$, ensuring signal rise time degradation below 10% and maintaining signal integrity.

5. Application case analysis and technical challenges

5.1. ESD protection schemes in consumer electronics

5.1.1. TVS integration case in mobile phone chip packaging

In 7 nm 5G baseband chip flip-chip packaging, multi-level TVS networks achieve coordinated optimization of ESD protection and signal integrity through layered architecture. First-level silicon-based TVS ($40\times60\ \mu m^2$) directly connects I/O pads via μBump arrays, controlling parasitic inductance at 0.3 nH while providing 8 kV HBM protection. Second-level GaAs TVS embedded in redistribution layers (RDL) suppresses 28 GHz high-frequency resonant noise. The overall scheme complies with IEC 61000-4-2:2024, withstanding 15 kV air discharge and adding only 0.8 dB insertion loss to USB 3.2 interfaces [6]. TVS layout strategy disperses ESD current paths, reducing peak current density from 1.2×10^6 A/cm^2 to 3.5×10^5 A/cm^2, with leakage current controlled below 0.3 μA, meeting EU dynamic monitoring standards for low power consumption and high reliability.

5.1.2. Miniaturization protection technology for wearable devices

Wearable devices integrate SiC TVS units into flexible polyimide (PI) substrates via three-dimensional heterogeneous integration, combined with nanoimprint processes to form 5 μm protective layers, achieving ultra-thin 0.48 mm packaging for miniaturization needs. Z-axis stacking compresses TVS area to 0.02 mm^2/I/O while maintaining 8 kV CDM protection. Device parameter optimization (dynamic resistance 0.8 Ω, junction capacitance 0.6 pF) significantly improves ECG sensor SNR by 6 dB, balancing ESD protection and signal quality. Reliability testing shows clamping voltage drift < 2% after 1000 bending cycles at 85% humidity, complying with JEDEC standards and suitable for TWS earphone chips < 10 mm in diameter, addressing core needs for miniaturized, high-reliability ESD protection in wearables.

5.2. High-reliability requirements in automotive electronics

5.2.1. ESD protection standards for automotive-grade chips (AEC-Q100)

Automotive-grade chip ESD protection must meet AEC-Q100-012 Rev-C:2023, focusing on TVS stability in extreme environments [7]. TVS must pass -40°C to 150°C temperature cycling and H3TRB tests, with clamping voltage drift < 5%. SiC-based TVS dynamic resistance increases 12% at 150°C, with leakage current below 0.5 μA. For 48V systems, TVS must withstand 80V pulses and 200 mJ avalanche energy, with WLP-integrated heat sinks controlling junction temperature within 175°C, complying with ISO 16750-2 and EU R155 regulations.

5.2.2. Multi-domain protection circuit design

Automotive electronics multi-domain protection requires coordinated optimization of power and signal domains. Power domain uses PMU cascaded with TVS, where TVS absorbs load dump energy (e.g., 100V/400 ms pulses in 48V systems) and PMU controls residual ripple to ± 200 mV. Signal domain targets 2.5 kV ESD impacts on FlexRay buses, using distributed TVS arrays and common-mode chokes to suppress noise > 40 dB [8]. This scheme

reduces vehicle EMC radiation by 6 dBμV/m, improving LIN bus error rate from 10^{-5} to 10^{-8}. Automotive Gigabit Ethernet TVS layout ensures differential pair capacitance imbalance < 0.1 pF, with LTCC design controlling transmission delay deviation to 0.5 ps/mm, meeting 1000BASE-T1 jitter requirements.

5.3. Technical challenges and solutions

5.3.1. TVS performance degradation in high-frequency scenarios

In high-frequency (> 30 GHz) scenarios, TVS parasitic inductance (0.5–2 nH) causes impedance mismatch and signal reflection, reducing response speed to > 2 ns. Specifically, 1 nH parasitic inductance at 60 GHz lowers ESD clamping efficiency by 60%, with residual voltage fluctuations ± 15%, significantly degrading signal integrity. To address this, three-dimensional stacked TVS uses TSV for vertical interconnection, shortening current paths to 200 μm and reducing parasitic inductance to 0.05 nH. Gradient permittivity materials optimize impedance matching, improving 28 GHz return loss by 8 dB. GaN-based TVS achieves dynamic resistance < 0.1 Ω at 140 GHz, meeting IEEE 802.3ck standards for 800 Gbps optical module ESD protection, enabling efficient energy discharge and signal integrity in high-frequency scenarios [9].

5.3.2. Trade-off between cost and reliability

In low-cost eWLB packaging, TVS performance is limited by low thermal conductivity and high dielectric loss of epoxy substrates. Embedding silicone composite heat dissipation layers (thermal conductivity 1.5 W/m·K) reduces TVS junction temperature from 125°C to 95°C, while laser trimming optimizes metal wiring, reducing protection costs by 40% [10]. Hybrid on-chip and discrete TVS integration elevates HBM levels from 4 kV to 10 kV at 15% BOM cost increase. China's Integrated Circuit Industry ESD Protection Technology Guideline (2023 Edition) requires consumer electronics protection cost ≤ 0.12 Chinese Yuan per kV, promoting flip-chip copper pillars over gold wire bonding, improving TVS integration yield to 98.5% while maintaining 8 kV CDM protection.

6. Conclusion

TVS integration technologies enhance ESD protection through three-dimensional stacking, multi-level protection, and new materials. TSV achieves response times < 0.3 ns, suitable for 5G; multi-level networks enable graded energy discharge, reaching 15 kV HBM protection. SiC and GaN extend operating temperatures to -55°C to 200°C, with withstand voltages > 30 kV. 28 nm chip CDM protection improves threefold, meeting 15 kV air discharge requirements. Future directions include two-dimensional materials like MoS_2 (response time 50 fs) for terahertz communications, and intelligent monitoring systems combining MEMS and machine learning, shifting ESD protection from passive to active prediction.

Disclosure statement

The author declares no conflict of interest.

References

[1] Zang J, 2015, The Hazards and Safety Prevention of Electrostatic Discharge (ESD) in Oil Depots. Water Fire Protection, 2015(4): 34–37.

[2] Wu J, 2013, Research on Integrated Circuit System Level ESD Protection, thesis, Zhejiang University.

[3] Li B, Li J, Gan X, et al., 2021, A System Level Packaging ESD Protection Technology. Microelectronics, 51(2): 211–215.

[4] Wu B, Tao W, Zhao Y, et al., 2017, Research on ESD Protection Method for Electronic Devices Based on TVS. Journal of Nanjing Normal University: Engineering Technology Edition, 17(2): 19–23.

[5] Sun H, Tong R, Xie W, 2014, Comparative Evaluation of TVS Protection Circuit and Capacitor Protection Circuit Based on Electrostatic Protection. Science and Technology Information, 12(33): 92–94.

[6] Liu C, Zhang F, He Y, et al., 2020, The Influence of BGA Packaging NC Pin on ESD Testing. Aerospace Electronics Technology, 51(3): 56–60.

[7] Cao Y, Wu Y, Yan X, et al., 2023, Research on the Applicability of AEC-Q100 Automotive Standard in High Reliability Field. China Standardization, 2023(10): 147–153.

[8] Zeng C, 2023, High-Energy Weapon Radio Frequency Three-Dimensional Heterogeneous Integration Technology in DARPA Electronics Revitalization Program. Journal of the Chinese Academy of Electronic Sciences, 18(4): 378–385.

[9] Wu H, 2010, IEC 61000-4-2:2008 Changes in Calibration Methods for Electrostatic Discharge Simulators. Safety and Electromagnetic Compatibility, 2010(1): 37–40.

[10] Qian T, 2011, Analysis of ESD Protection Design for Electronic Communication Products. Enterprise Technology Development: Second Half, 30(12): 8–9.

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