Journal of Electronic Research and Application, 2025, Volume 9, Issue 3
http://ojs.bbwpublisher.com/index.php/JERA
ISSN Online: 2208-3510
ISSN Print: 2208-3502

Research on Innovative Design and Preparation Technology of Power Integrated Isolation Structure

Yili Xu*, Xin Li, Xiaodong Yin, Guowei Zhang, Jingyi Li, Qianqian Liu

Hangzhou Puxi Optoelectronic Semiconductor Technology Co., Ltd., Hangzhou 311700, Zhejiang, China

**Author to whom correspondence should be addressed.*

Abstract: Power integrated isolation structures play a crucial role in the field of power electronics, especially in silicon carbide (SiC) devices, where challenges such as high leakage current and insufficient voltage endurance are prevalent. This paper introduces a novel isolation technology based on vanadium ion implantation, achieving high-performance SiC monolithic integration through deep energy level trapping engineering and three-dimensional composite isolation design. The core technologies include: semi-insulating layer + dielectric trench co-isolation, high-precision process control, high-temperature compatibility optimization, ultra-high breakdown field strength, support for 10kV class IGBT/MOSFET integration, and a 30–50% increase in chip area utilization, combining high performance with low-cost advantages.

Keywords: Silicon carbide; Power integration; Full enclosure isolation; Vanadium ion injection; Dielectric backfilling

Online publication: 5 June, 2025

1. Introduction

In today's rapidly evolving field of power electronics, the innovative design and preparation technology of power integrated isolation structures as key components have become particularly important. With the increasing demands for energy conversion efficiency and the trend towards miniaturization in electronic devices, higher performance requirements are placed on power-integrated isolation structures [1–4]. Moreover, with the rapid development of areas such as electric vehicles and renewable energy generation systems, the role of power-integrated isolation structures in these applications has become increasingly prominent. Therefore, researching power-integrated isolation structures holds theoretical innovation value and has profound practical significance. It can provide technical support to related industries, promote advancements in energy conversion technology, and positively impact environmental protection and sustainable development [5–7].

With the rapid development of power electronics technology, power integrated isolation structures, as key components, are advancing towards higher efficiency, smaller size, and greater reliability. In this process, power-integrated isolation structures play a crucial role. They not only effectively isolate high-voltage and low-voltage

circuits to ensure safe operation of equipment but also reduce energy loss through optimized design, thereby improving the overall system's energy efficiency ratio. On the technical front, the introduction of new materials such as silicon carbide (SiC) and gallium nitride (GaN) has significantly enhanced the performance of power integrated isolation structures. These materials offer higher thermal conductivity and electric field strength, enabling the isolation structure to operate under more extreme conditions while maintaining low heat dissipation. Additionally, advancements in microelectronics manufacturing technologies, such as the refinement of lithography and etching techniques, have allowed for further miniaturization of isolation structures, leading to more compact circuit designs. In terms of application, power-integrated isolation structures are being widely used in areas like electric vehicles, renewable energy conversion systems, and industrial automation [8–12].

With the rapid development of new energy vehicles, industrial frequency conversion, and aerospace technology, power semiconductor devices are evolving towards higher frequencies, higher voltages, and greater integration. Single-chip power integration technology, by integrating power devices with drive/control circuits on a single chip, can significantly reduce parasitic parameters and improve system efficiency, making it a core direction for the next generation of power electronic systems. In the silicon-based semiconductor field, dielectric isolation DI technology achieves electrical isolation between devices through SiO_2/Si_3N_4 composite layers, with a breakdown field strength reaching up to 10 MV/cm, widely applied in high-performance integrated circuits [13–15]. However, the vertical device structure of SiC leads to the failure of traditional SoI (Silicon on Insulator) technology, presenting the following challenges: First, the limitations of PN junction isolation: silicon-based PN junction isolation relies on impurity diffusion or ion implantation to form depletion layers, but the high critical breakdown electric field of SiC materials requires an injection depth exceeding 3 μm. Commercial ion implanters have an energy limit of only 1.5 MeV, resulting in an effective injection depth of less than 1.5 μm, as shown in **Figure 1**. In addition, the parasitic NPNP structure at the PN junction interface is prone to latch-up effects at high temperatures; secondly, the lattice mismatch issue of dielectric isolation: when SIMOX (Separation by Implanted Oxygen) technology introduces SiO_2 dielectric in SiC, the lattice mismatch reaches 19%, leading to an interface defect density as high as $10^{13}cm^{-2}$, significantly increasing leakage current [16–19], as shown in **Figure 2**.

This study innovatively proposes a synergistic isolation mechanism between the semi-insulating layer and the dielectric trench, breaking through existing bottlenecks through the following technical approaches: First, deep energy level trap engineering: selecting vanadium as a deep energy level dopant, forming a compensatory semi-insulating region through high-temperature annealing [19–21]; Second, using a three-dimensional isolation architecture: a bottom semi-insulating layer with a depth of 3–5 μm and side wall dielectric trenches with a thickness of 0.5 μm SiO_2 to form a fully enclosed barrier; Third, process compatibility optimization: all process steps have temperatures <1800°C, seamlessly integrating with existing SiC MOSFET process technology.

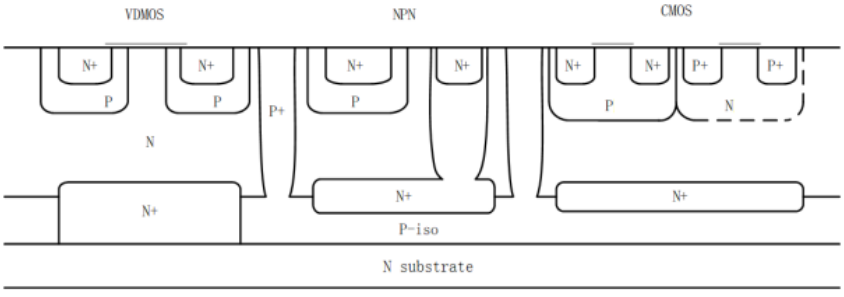

Figure 1. Schematic diagram of a power integrated circuit structure isolated by PN junction

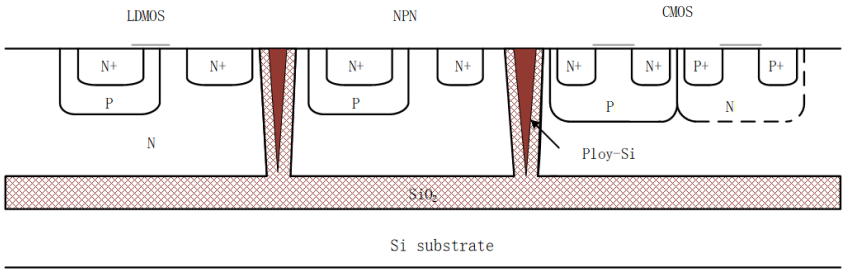

Figure 2. Schematic diagram of power integrated circuit structure with medium isolation

2. Advanced isolation structures for high-temperature and high-power silicon carbide devices

In high-temperature and high-power applications of wide-bandgap semiconductor silicon carbide devices, traditional isolation structures often face issues such as increased leakage current, reduced voltage endurance, and insufficient thermal stability. To address these challenges, new isolation structures achieve electrical isolation between devices through innovative material engineering and process design from vertical, bottom, lateral, and sidewall dimensions, as shown in **Figure 3**.

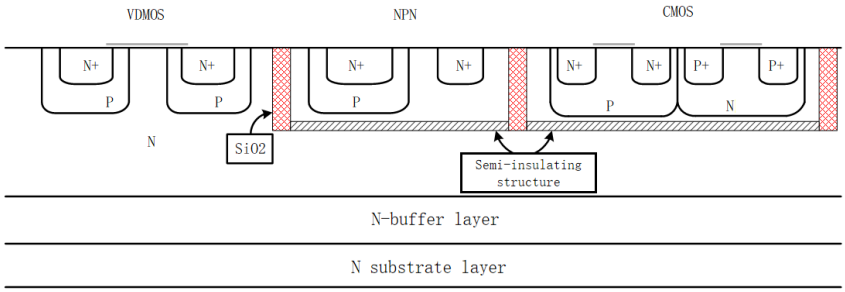

Figure 3. Schematic diagram of power integrated isolation structure

The specific principle is as follows:

(1) Vertical isolation: Vanadium plasma injection forms a semi-insulating layer

On the surface of the SiC substrate, vanadium plasma is introduced by ion implantation technology to form a semi-insulating layer with high resistivity, to realize the electrical isolation between the surface device and the bottom circuit. The core design principles include:

Material selection and band modulation: Vanadium acts as a deep-level impurity in SiC, introducing defect states into the bandgap, such as vanadium substitution defects V_Si or V_C, significantly increasing the material's resistivity. This semi-insulating property stems from the strong trapping effect of deep-level traps on carriers, effectively blocking vertical leakage current paths.

Injection process optimization: By precisely controlling the energy and dose of vanadium ion injection, combined with subsequent high-temperature annealing to repair lattice damage, a uniform and stable semi-insulating region can be formed on the SiC surface. The annealing process also activates the deep energy level characteristics of vanadium, avoiding reliability degradation due to lattice disorder.

Voltage endurance and thermal stability: The high breakdown field strength of the semi-insulating layer is >3 MV/cm, which can withstand the longitudinal high voltage difference during device operation, and its SiC wide band gap characteristics can maintain excellent insulation performance at high temperature, avoiding the reliability degradation caused by thermal carrier injection in the traditional SiO_2/SiN dielectric layer.

This design breaks through the limitations of traditional PN junction or dielectric isolation in high voltage and high temperature scenarios, especially suitable for SiC power MOSFET, JFET, and other devices, can greatly reduce the substrate leakage current and improve the blocking voltage capability.

(2) Side wall isolation: A composite structure of medium isolation or multiple methods

To realize lateral isolation between surface devices and adjacent devices, the new structure adopts medium isolation, PN junction isolation, semi-insulation isolation, or its combination scheme. The specific working principle is as follows:

Dielectric isolation SiO_2/SiN: A high dielectric strength dielectric layer is deposited on the sidewall of the device to suppress lateral leakage by physical barrier and electric field shielding effect. This method is compatible with standard CMOS process, but the stress matching of the dielectric layer needs to be optimized to avoid interface cracking at high temperature.

PN junction isolation: In the sidewall region, p-type or n-type doped regions are formed through ion implantation, creating an inverse-bias PN junction with the opposite doping type to adjacent devices. Electrical isolation is achieved by utilizing the depletion layer expansion. For example, Al+ is implanted into the sidewall of an n-type SiC device to form a p-type isolation ring. Under reverse bias, the width of the depletion layer can reach several micrometers, effectively blocking lateral leakage.

Extension of semi-insulating isolation: The process of injecting vertically isolated vanadium into the side wall region is extended to form a continuous semi-insulating wrapping layer. The semi-insulating layer can be covered over the three-dimensional surface of the device using inclined ion injection or secondary injection after etching, achieving full enclosure isolation.

Advantages of the combination scheme: For different voltage levels and spatial constraints, a “dielectric layer + PN junction” dual-layer isolation can be adopted, where the dielectric layer bears the main voltage withstand capability, and the PN junction provides auxiliary depletion or a “semiconductor layer + dielectric layer” composite structure that balances high voltage withstand and process compatibility. For example, in a 10kV SiC IGBT, the side walls use a combination of a 2μm SiO_2 dielectric layer and a p-type isolation ring, achieving lateral voltage withstand >12kV within a limited area.

3. Preparation method

Preparation of vertical isolation layer: Vanadium plasma injection to form a semi-insulating layer

(1) SiC Pre-treatment, use RCA standard cleaning process to remove surface organic pollutants and metal ions, followed by the removal of native oxide with DHF solution.

(2) Deposit a layer of oxide film, and then go through photolithography, etching, de-gelling, and other processes to obtain the injection hard mask with the required isolation area (**Figure 4**).

(3) Vanadium ion injection, using a high-energy ion injector to adjust according to the target injection depth, usually needs to penetrate the device active area to the substrate interface below 0.5–2 μm (**Figure 5**).

(4) The active area is messy.

(5) High temperature annealing activation, use a heating furnace to perform high temperature annealing in an Ar atmosphere to avoid surface oxidation and ensure lattice damage repair and vanadium deep energy level activation (**Figure 6**).

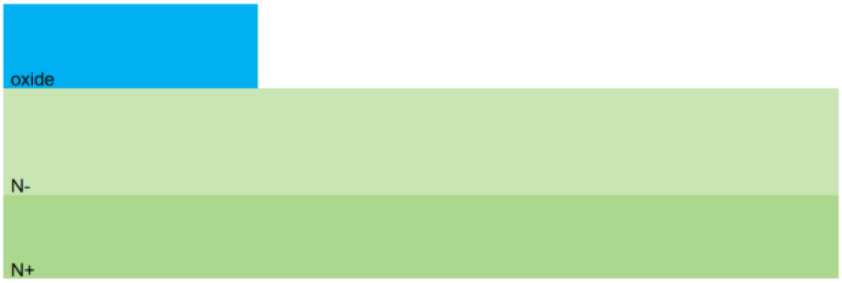

Figure 4. Schematic diagram of the isolation area

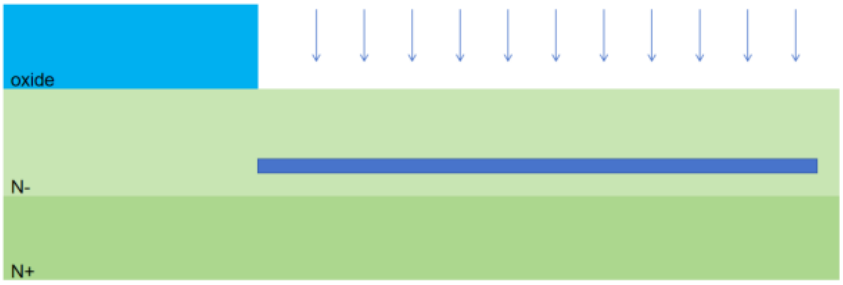

Figure 5. Schematic diagram of vanadium ion injection in the isolation zone

Figure 6. Schematic diagram of the active area after chaos

Preparation of side wall isolation structure: Take the medium process as an example

(1) Deposit a layer of oxide film, and then go through photolithography, etching, de-gelling, and other processes to obtain the etching hard mask that needs to isolate the sidewall region; or a single-step photolithography process to obtain the etching hard mask that needs to isolate the sidewall region.

(2) Device platform etching, the etching depth is the maximum concentration of injected vanadium ions, forming the side wall structure of the device isolation area (**Figure 7**).

Figure 7. Schematic diagram of the isolation zone groove

(3) Side wall isolation layer deposition, medium isolation SiO_2 or SiN (**Figure 8**).

Figure 8. Schematic diagram of the filling medium in the isolation zone tank

Key process advantages:

(1) High precision control: The depth and concentration gradient of the semi-insulating layer can be controlled by energy and dose adjustment.

(2) High temperature compatibility: The annealing process is seamlessly connected with the manufacturing process of SiC devices to avoid additional thermal budget.

(3) Three-dimensional full enclosure isolation: The inclined injection and combination process ensure that the device side wall and bottom are fully electrically isolated.

4. Conclusion

Silicon carbide (SiC) devices face challenges such as high leakage current and insufficient voltage endurance in high-power applications. A new isolation technology based on vanadium (V) plasma injection, combined with composite isolation design, has achieved a core breakthrough in high-performance SiC monolithic integrated circuits:

(1) Deep energy level trap to improve vertical isolation: After vanadium injection into SiC, a deep energy level donor/receptor (V_Si or V_C) is formed, and the resistivity is increased to 10^8–10^{12} Ω·cm by capturing carriers, and the breakdown field strength exceeds 3 MV/cm.

(2) Low damage process guarantees performance: The high energy injection and high temperature annealing are optimized, the lattice defect can be reduced by 90%, and the carrier mobility can be restored to 90% of the original SiC.

(3) Three-dimensional composite isolation structure: The vertical vanadium injection semi-insulating layer is combined with the side wall medium SiO_2 or SiN and PN junction isolation, which is used to realize the SiC monolithic integrated circuit based on the vertical structure high-power devices and circuits, supporting 10kV level IGBT/MOSFET monolithic integration, and the power density exceeds 200 W/cm^3.

(4) Low cost: The process is compatible with existing SiC production lines, and no additional equipment is required.

(5) Small area occupation: The three-dimensional isolation structure improves the chip area utilization by 30–50% through the cooperative design of semi-insulating layer and medium/PN junction.

Based on vanadium plasma implantation, a new isolation technology has been developed. By employing deep-level trap engineering and multi-dimensional composite isolation design, it addresses the isolation bottleneck of SiC devices in high-power and high-temperature scenarios, offering advantages of high performance, high reliability, and low cost. The process compatibility and small-area characteristics further accelerate the commercialization of SiC monolithic integrated circuits, providing core technological support for next-generation

power electronic systems in fields such as new energy, smart grids, and aerospace. The successful application of this technology will drive the wide-bandgap semiconductor industry toward higher power density and more extreme environmental adaptability.

Disclosure statement

The authors declare no conflict of interest.

References

[1] Zhou L, 2025, The Hong Kong Stock Exchange Welcomed —— Han Tiancheng, The World's Leading Epitaxial Chip Leader, China Securities Journal, April 9, 2025, (A07).

[2] Xu T, 2025, A Rapid Journey to New Efforts, Chizhou Daily, January 28, 2025, (001).

[3] Feng Q, Zhang Y, 2025, Watering the "Rainforest of Science and Technology Innovation" with Patience, All-Sectors Herald, January 24, 2025, (003).

[4] Yang P, 2025, The Expansion Wave Surges, and Silicon Carbide is Poised to Move Forward Again, China Electronics News, January 10, 2025, (007).

[5] He X, 2024, Pengpai "Core" Kinetic Energy Rises to the "Core" High Ground, Chizhou Daily, December 27, 2024, (001).

[6] Wei P, Shen S, Shen T, 2024, Qianwan New Area Accelerates the "Chip" Journey, Ningbo Daily, December 12, 2024, (004).

[7] Luo Y, 2025, Price and Market Game: Silicon Carbide Chip Accelerates into the Race for Positioning, 21st Century Business Herald, April 17, 2025, (010).

[8] Gu Y, 2025, Industrial Application of Silicon Carbide Becomes a New Blue Ocean, Economic Daily, April 16, 2025, (006).

[9] Xu Z, 2025, Three New Semiconductor Materials Prepare for Industrialization, China Electronics News, March 21, 2025, (007).

[10] Zheng J, Li Z, Zhang C, et al., 2025, Research Progress on the Design and Reliability Evaluation Technology of Third-generation Semiconductor Packaging Structure. Electronics and Packaging, 25(03): 36–50.

[11] Luo Y, 2025, The Elimination of Silicon Carbide: Price Competition, Giant Adjustment, 21st Century Business Herald, January 23, 2025, (010).

[12] Liao S, Xie Q, Jiang Q, 2025, A Brief Discussion on the Application Status and Prospects of Semiconductor Materials in the Third Generation. China Integrated Circuit, 34(Z1): 34–39.

[13] Zhu Q, 2013, SiO2/SiC Interface Transition Zone and Plasma Passivation Process Research, dissertation, Dalian University of Technology.

[14] Hu C, Liu J, Liu Q, et al., 2025, SiC MOS Analysis Method of Passivation Effect of Interface Defects in Capacitor Oxide Layer. Semiconductor Technology, 2025: 1–7.

[15] Pan E, 2023, Research on Key Technologies of 4H-SiC MOS Gate Oxygen Interface Passivation, dissertation, Xidian University.

[16] Zhang Y, Wei S, Ding P, et al., 2023, Structural and Electrical Properties Evolution of Carbon Defects at the SiC/SiO2 Interface under Bending Stress. Research and Progress in Solid-State Electronics, 43(03): 208–213.

[17] Lin Y, 2023, Research on SiC MOSFET Degradation Behavior for Failure Prediction, dissertation, South China University of Technology.

[18] Wang Z, Wu Q, 2016, Overview of SOI Patent Technology. Henan Science and Technology, (08): 64–66.

[19] Zhang B, 2014, Study on Ionizing Radiation Effects of Oxygen-isolated SOI Materials, dissertation, Jinan University.

[20] Wang C, Zhang Y, Zhang Y, et al., 2008, Annealing Effect of Semi-insulating SiC Prepared by Vanadium Injection. Electronic Devices, (03): 770–775.

[21] Wang C, Zhang Y, Zhang Y, 2006, Study on the Semi-insulating Characteristics of 4H-SiC After Vanadium Injection. Journal of Semiconductor Science, (08): 1396–1400.