Journal of Electronic Research and Application, 2025, Volume 9, Issue 2
http://ojs.bbwpublisher.com/index.php/JERA
ISSN Online: 2208-3510
ISSN Print: 2208-3502

A Study on the Modeling and Design of Sigma-Delta Modulator for High Precision ADC

Haodong Guo, Longyu Li, Xia Zhang*

Shandong Provincial Key Laboratory of Optical Communications Science and Technology, School of Physics Science and Information Engineering, Liaocheng University, Liaocheng 252000, Shandong, China

***Corresponding author:** Xia Zhang, wenerzhang2002@163.com

Abstract: With the continuous improvement of signal processing accuracy requirements in modern electronic systems, the demand for high-precision analog-to-digital converters (ADCs) is increasing. Sigma-Delta modulator, as the most important component of high-precision ADC, is widely used in high-quality audio, high-precision instrument measurement, and other fields due to its advantages of high precision, strong noise resistance, and low hardware cost. This article designs a discrete structure third-order four-bit high-precision Sigma-Delta modulator through modeling, with an oversampling rate set to 512. Under ideal conditions, the simulation results show that the SDNR reaches 152.7db and the ENOB is 25.24bits. After introducing non-ideal noise, the system performance has decreased. The simulation results show that the SDNR is as high as 124.5db and the ENOB is 20.39bits. This indicates that the design can achieve high-precision conversion and provide assistance for further research in the future.

Keywords: Analog-to-digital converter; Sigma-Delta modulator; High precision; Modeling design

Online publication: April 3, 2025

1. Introduction

With the rapid development of modern electronic technology, high-precision analog-to-digital converters (ADCs) are increasingly widely used in key fields such as audio processing, wireless communication, and precision measurement [1]. High-precision ADCs not only have the advantages of high accuracy, good linearity, and low quantization noise but also have strong anti-interference ability and easy integration with digital circuits [2]. Through the strategy of exchanging speed for accuracy, they can achieve high-resolution analog-to-digital conversion at a lower complexity than analog circuits. Although high-precision ADCs have many advantages, their design also faces many challenges [3]. Especially in the pursuit of higher precision and lower power consumption, it is necessary to comprehensively consider the effects of modulator structure, circuit implementation, and non-ideal factors [4]. As the most important component of Sigma-Delta ADCs, the design of Sigma-Delta modulators directly affects the effectiveness and reliability of the system [5]. Therefore, researching

and designing high-precision modulators plays an important role in high-precision ADCs. Taking into account accuracy, power consumption, error, and linearity, this paper designs a Sigma-Delta modulator that achieves high-quality factor through system modeling and simulation [6].

2. Ideal modulator design

2.1. Modulator design process

In the modeling and design process of high-precision Sigma-Delta modulators, the first step is to determine the design specifications based on the application, select the appropriate system topology structure according to the requirements applicable to the audio field, and complete the system-level modeling. Then, each coefficient is determined based on the calculation, and reasonable scaling is completed according to the circuit design requirements [7]. It is necessary to determine whether the system is stable based on the zero pole diagram, integrator current, and other conditions. When the system is stable, an ideal model simulation can be performed to check whether the simulation indicators meet the actual requirements [8]. After the system simulation is completed, non-ideal factors are analyzed and introduced, and key noise parameters are set to supplement the overall model for simulation verification. The impact of non-ideal factors on the system is examined to provide further guidance for achieving circuit-level design [9].

2.2. Topology structure selection

The main performance parameters of the modulator are signal-to-noise distortion ratio and dynamic range. The following formula is used to calculate the signal-to-noise distortion ratio of the modulator:

$$\mathrm{SQNR} = 6.02N + 1.76 + (20L + 10)\log(\mathrm{OSR}) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) \tag{1}$$

Among them, N is the quantization bit number of the modulator, L is the modulator order, and OSR is the oversampling multiple [10]. According to formula (1), the Sigma-Delta modulator is mainly related to the integrator order, quantization bit number, and oversampling rate. Next, calculate the dynamic range of the modulator:

$$\mathrm{DR(dB)} = 10\lg\left(\frac{P_{sig,out,max}}{IBN}\right) \approx 10\lg\left[\frac{3}{2}\left(2^N - 1\right)^2 \frac{(2L+1)\mathrm{OSR}^{(2L+1)}}{\pi^{2L}}\right] \tag{2}$$

Among them, the output power of the P_ (sig, out, max) signal and IBN are the in band noise power. As shown in Equation (2) above, the higher the order of the modulator, the stronger its ability to suppress quantization noise within the bandwidth, the higher the signal-to-noise ratio, and the higher the accuracy. It can be seen that selecting a high-order structure significantly improves the performance of the modulator, effectively reducing noise and power consumption. However, considering that high-order structures can cause poor system stability, a third-order structure is selected and the system stability is ensured by setting an appropriate transfer function [11].

As the number of quantization bits increases, the multi-bit quantizer structure becomes more stable, and the performance of the modulator approaches that of an ideal modulator [12]. Therefore, in this design, a four-bit quantizer structure is ultimately chosen to improve the performance of the modulator. In a feedback modulator,

the input terminals of each integrator are affected by the feedback DAC, while in a feedforward modulator, only the input terminal of the first integrator is affected by the DAC [13]. Considering the requirement for high precision and not too high speed, the feedforward CIFF structure was ultimately chosen. The final modulator model is established as shown in **Figure 1**:

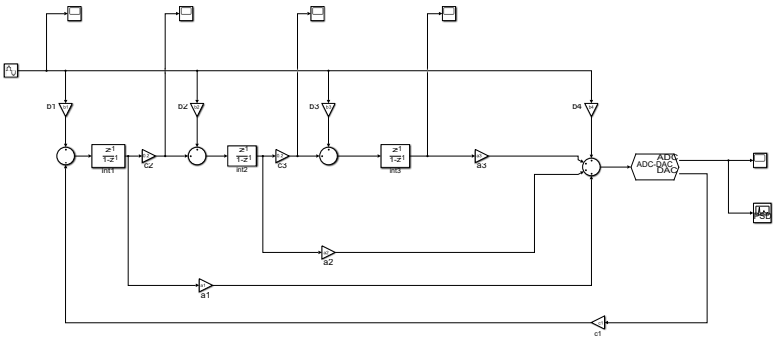

Figure 1. Structure model of third-order four-bit CIFF modulator

2.3. Modulator coefficient optimization and system simulation

After completing Simulink modeling, use functions such as scale in MATLAB toolbox to scale the modulator coefficients, taking into account signal dynamic range, noise shaping efficiency, and system stability. Through theoretical analysis and tool assistance, achieve proportional scaling before and after coefficients. After continuous optimization of various coefficients, the final optimized coefficients were obtained and compared with the initial coefficients as shown in **Table 1**.

Table 1. Comparison of modulator coefficient optimization before and after

Coefficient	a1	a2	a3	b1	b2	b3	b4	c1	c2	c3	g
Initial value	1.8183	2.2305	1.2085	0.2988	0	0	1	0.2988	0.3750	0.1994	0
Final value	3.5	5	3	0.2	0	0	1	0.2	0.2	0.2	0

After obtaining the preliminary optimized modulator coefficients, the zero pole distribution of the system was calculated using MATLAB tools. **Figure 2** illustrates the zero pole distribution of the system.

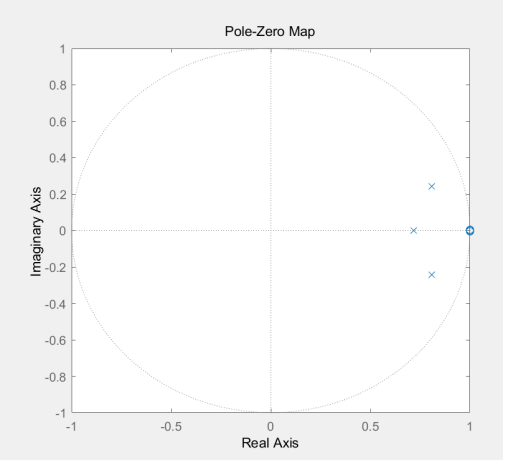

Figure 2. Distribution of zero and pole points in the system

From **Figure 2**, it can be seen that in the zero pole diagram of the noise transfer function, the zeros of the transfer function are separated from each other and all are at z = 1, and all the poles are located within the unit circle. Therefore, it can be concluded that the system remains stable. Next, the optimized coefficients are used to simulate the system. Under the condition of setting the input as a sine signal, the output spectrum of the ideal third-order four-bit CIFF modulator Simulink model is shown in **Figure 3**.

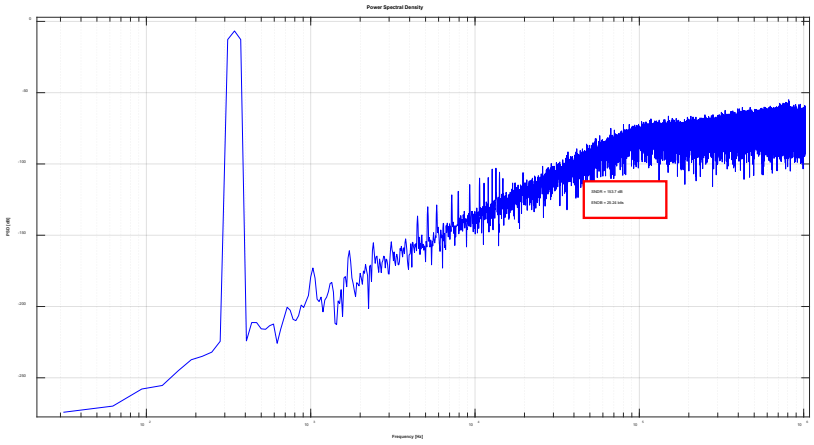

Figure 3. Simulation diagram of ideal modulator

From **Figure 3**, it can be seen that under ideal conditions, the SNDR of the modulator is 153.7dB, with an effective bit count of approximately 25.24bits, which meets the design requirements. In addition, the stability of the output signal can be observed based on the oscilloscope on each integrator. **Figure 4** shows the output results of each level of integrator. It can be seen that the outputs of all levels of integrators are within 0.6V, and there is no overload phenomenon, so the circuit current remains stable, which further proves the stability of the system.

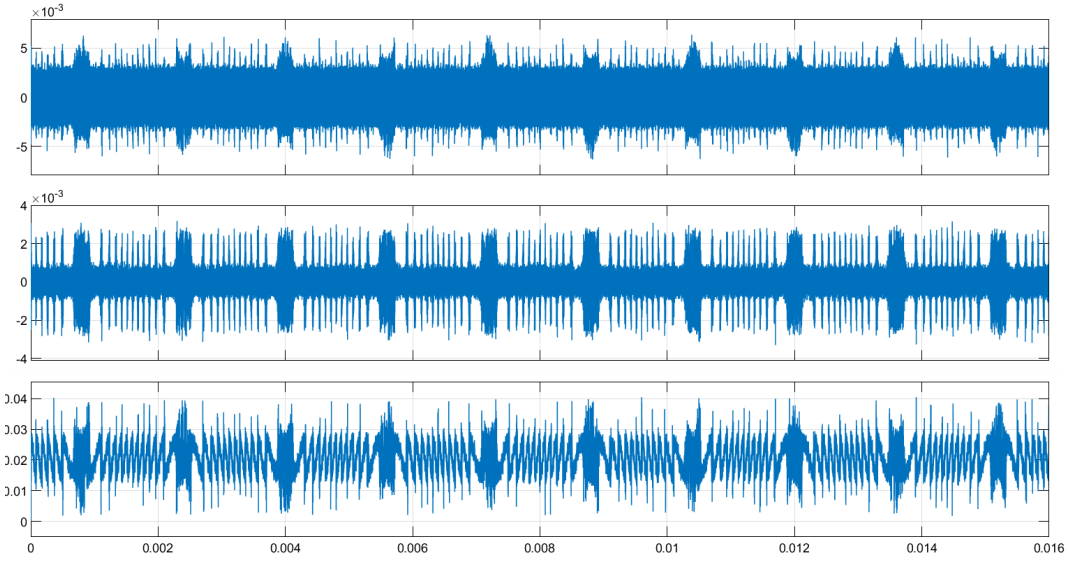

Figure 4. Output of integrators at all levels

3. Complete topology structure

Non-ideal factors and nonlinearity in circuits can reduce the performance of modulators, and these non-ideal

factors affect the quality factor of modulators through their own properties, the influence of specific circuits, and their impact on the noise transfer function. At the input of the modulator, non-ideal factors can be modeled as additive noise sources, and this structure mainly considers independent topology thermal noise. The thermal noise of the switch is mainly related to the sampling capacitor, and the impact of kT/C thermal noise on the in band noise IBN is as follows:

$$IBN_{\frac{KT}{C}} \approx \frac{4KT}{C_S OSR} \tag{3}$$

Among them, K represents Boltzmann constant, T represents absolute temperature, C-S represents sampling capacitance, and OSR is oversampling rate. Research has found that the in band noise generated by kT/C is similar to the in band noise contribution of rational quantization noise. Therefore, a non-ideal model incorporating kT/C noise is shown in **Figure 5**.

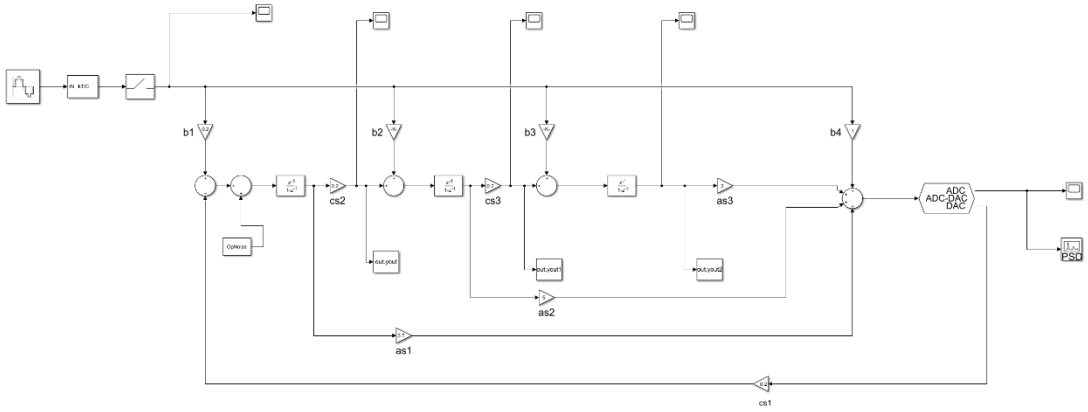

Figure 5. Introduction of non-ideal factor modulator model

According to the design requirements, taking into account the trade-off between actual circuit design and system performance, a clock jitter of 0.5ns, a sampling capacitor of 6 pf, an operational amplifier gain of 60dB, an operational amplifier voltage swing rate of 10V/us, and a sine input signal swing amplitude of 0.8V were ultimately selected. Set the above factors in the system and simulate the modulator as a whole. The simulation results are shown in **Figure 6**:

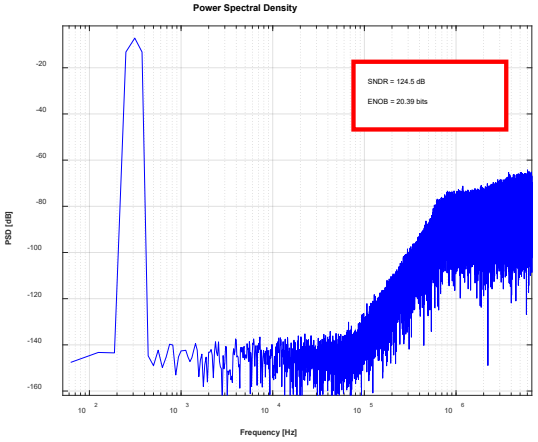

Figure 6. Overall performance simulation results of modulator

According to the simulation results in **Figure 6**, the SNDR with the addition of a non-ideal factor modulator is reduced to 124.5dB, and the effective bit count is reduced to 20.39 bits. This indicates that the influence of non-ideal factors cannot be ignored in practical design, but there is a margin left in the design process to achieve the expected design goals.

4. Conclusion

This article designed a high-precision Sigma-Delta modulator system, which adopts a third-order four-bit quantized CIFF structure with an oversampling rate of 256 and improves system performance by adjusting coefficients. After incorporating non-ideal factors, although the overall performance of the system decreased, the simulation results met expectations. The final simulation results showed that SNDR could reach 124.5dB and ENOB could reach 20.39bits, which meets the expected design goals and is helpful for further circuit design. It can be applied to the field of audio signal conversion.

Disclosure statement

The authors declare no conflict of interest.

References

[1] He B, Guo X, Jia H, et al., 2025, A 100-MHz Bandwidth Continuous-Time Sigma-Delta ADC with 1 V Supply in 28 nm CMOS. Microelectronics Journal, 158: 106597.

[2] Li W, Tian D, Zhu H, et al., 2025, A Programmable Gain Amplifier Featuring a High Power Supply Rejection Ratio for a 20-Bit Sigma-Delta ADC. Electronics, 14(4): 720.

[3] Kohandel R, Yavari M, 2025, A Systematic Time-Based approach for Analysis and Compensation of Excess Loop Delay in Continuous-Time Sigma-Delta Modulators Exceeding One Clock Cycle. Results in Engineering, 25: 103912.

[4] Ye M, Liu Z, Zhao Y, 2024, Design of a Sigma-Delta Analog-to-Digital Converter Cascade Decimation Filter. Electronics, 13(11): 2090.

[5] Brandon M, 2024, Orbital Angular Momentum Small-X Evolution: Exact Results in the Large-Nc Limit. Journal of High Energy Physics, 2024(4): 55.

[6] Wang J, Wang G, Li K, et al., 2024, Erratum: A 1.8 V 115.52 dB Third-Order Discrete-Time Sigma-Delta Modulator Using Nested Chopper Technology. Journal of Circuits, Systems and Computers, 33(09): 2492001.

[7] Khachi CS, Wanas KA, 2024, Two Families of m-fold Symmetric Bi-univalent Functions Involving a Linear Combination of Bazilevic Starlike and Convex Functions. Earthline Journal of Mathematical Sciences, 14(3): 405–419.

[8] Dong S, Ning S, Yuan M, et al., 2024, A Low-Power Sigma-Delta Modulator Based on High-Order Op-Amp Sharing Technique for Speech Communication. AEUE - International Journal of Electronics and Communications, 176: 155116.

[9] Wang J, Wang G, Li K, et al., 2024, A 1.8 V 115.52 dB Third-Order Discrete-Time Sigma-Delta Modulator Using Nested Chopper Technology. Journal of Circuits, Systems and Computers, 33(07): 2450126.

[10] Chen K, Chen M, Cheng L, et al., 2022, A 124 dB Dynamic Range Sigma-Delta Modulator Applied to Non-Invasive

EEG Acquisition Using Chopper-Modulated Input-Scaling-Down Technique. Science China Information Sciences, 65(4): 140402.

[11] Ocampo-Hidalgo JJ, Castillo JA, Molinar-Solis JE, 2022, Processing Electrocardiographic Signals Using a Custom Designed Sigma-Delta Modulator. Journal of Circuits, Systems and Computers, 31(03): 2250040.

[12] Nikolaos G, Alkis PH, 2022, Functional Verification of a Sigma-Delta ADC Real Number Model. International Journal of Electronics, 109(1): 119–134.

[13] Toshihiro I, Shoji M, Yoshiya K, 2022, Sigma-Delta Beamformer DOA Estimation for Distributed Array Radar. IEICE Transactions on Communications, E105.B(12): 1589–1599.